WM5102

Audio Hub CODEC with Voice Processor DSP

DESCRIPTION

The WM5102[1] is a highly-integrated low-power audio system for smartphones, tablets and other portable audio devices. It combines wideband telephony voice processing with a flexible, high-performance audio hub CODEC.

The WM5102 digital core provides a powerful combination of fixed-function signal processing blocks with a programmable DSP. These are supported by a fully-flexible, all-digital audio mixing and routing engine with sample rate converters, for wide use-case flexibility. The programmable DSP supports a range of audio processing software packages (supplied separately); user-programmed solutions can also be supported. Fixed-function signal processing blocks include filters, EQ, dynamics processors and sample rate converters.

A SLIMbus interface supports multi-channel audio paths and host control register access. Multiple sample rates are supported concurrently via the SLIMbus interface. Three further digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample rate detection enables seamless wideband/narrowband voice call handover.

Two stereo headphone drivers each provide stereo ground-referenced or mono BTL outputs, with noise levels as low as $2.3\mu V_{RMS}$ for hi-fi quality line or headphone output. The CODEC also features stereo 2W Class-D speaker outputs, a dedicated BTL earpiece output and PDM for external speaker amplifiers. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the Class-D speaker output, or via an external driver on the PDM output interface. All inputs, outputs and system interfaces can function concurrently.

The WM5102 supports up to six microphone inputs, each either analogue or PDM digital. Microphone activity detection with interrupt is available. A smart accessory interface supports most standard 3.5mm accessories. Impedance sensing and measurement is provided for external accessory and push-button detection.

The WM5102 power, clocking and output driver architectures are all designed to maximise battery life in voice, music and standby modes. Low-power 'Sleep' is supported, with configurable wake-up events. The WM5102 is powered from a 1.8V external supply. A separate supply is required for the Class D speaker drivers (typically direct connection to 4.2V battery).

Two integrated FLLs provide support for a wide range of system clock frequencies. The WM5102 is configured using the I2C, SPI or SLIMbus interfaces. The fully-differential internal analogue architecture, minimal analogue signal paths and on-chip RF noise filters ensure a very high degree of noise immunity.

FEATURES

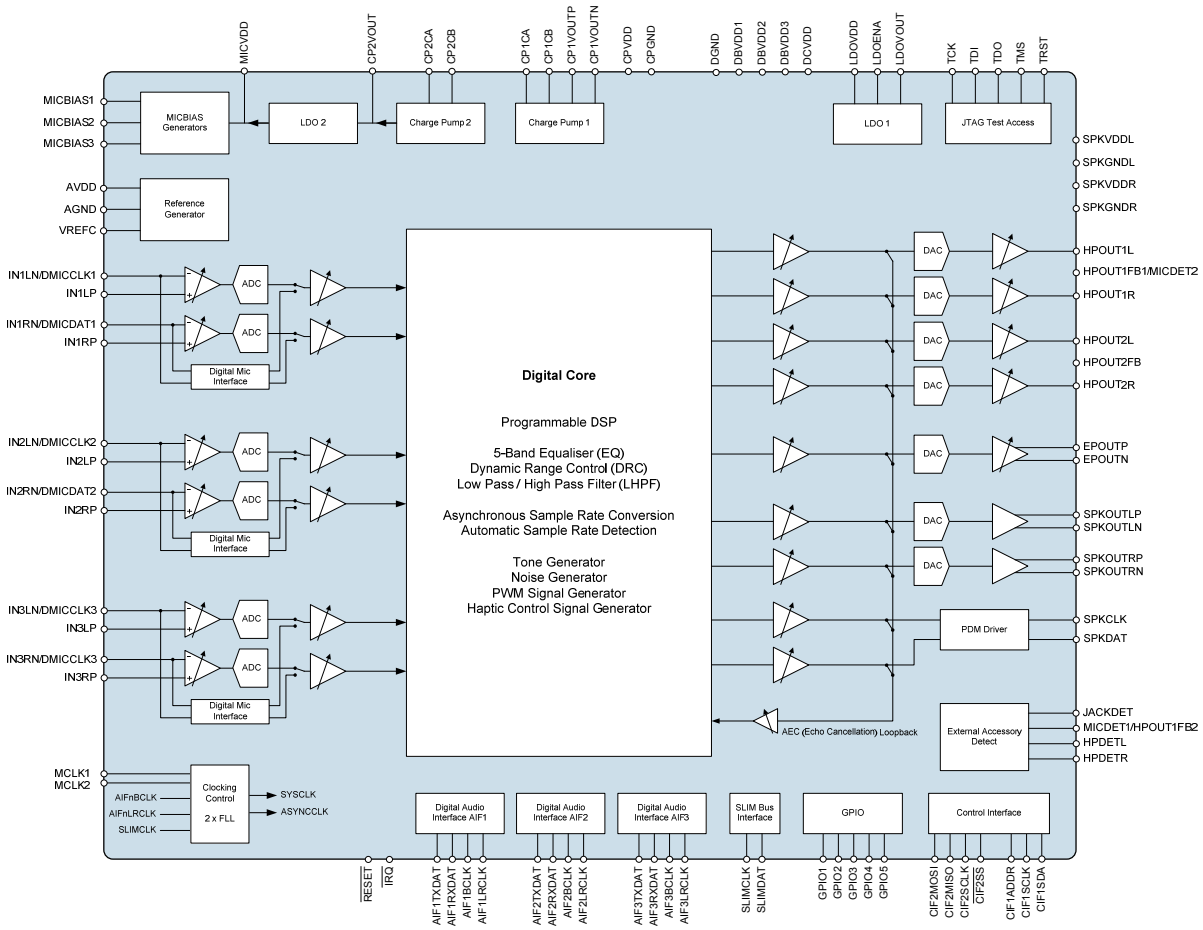
- Audio hub CODEC with integrated voice processor DSP
- Programmable DSP capability for audio processing
- Fixed function signal processing functions
  - Wind noise, sidetone and other programmable filters
  - Dynamic Range Control, Fully parametric EQs
  - Tone, Noise, PWM, Haptic control signal generators
- Multi-channel asynchronous sample rate conversion
- Integrated 6/7 channel 24-bit hi-fi audio hub CODEC
  - 6 ADCs, 96dB SNR microphone input (48kHz)
  - 7 DACs, 113dB SNR headphone playback (48kHz)
- Audio inputs
  - Up to 6 analogue or digital microphone inputs
  - Single-ended or differential mic/line inputs
- Multi-purpose headphone / earpiece / line output drivers
  - 2 stereo output paths
  - 29mW into 32Ω load at 0.1% THD+N
  - 100mW into 32Ω BTL load at 5% THD+N
  - 6.5mW typical headphone playback power consumption
  - Pop suppression functions
  - $2.3\mu V_{RMS}$ noise floor (A-weighted)
- Mono BTL earpiece output driver
- 2 x 2W stereo Class D speaker output drivers
  - Direct drive of external haptics vibe actuators
- Two-channel digital speaker (PDM) interface
- SLIMbus® audio and control interface
- 3 full digital audio interfaces
  - Standard sample rates from 4kHz up to 192kHz
  - Ultrasonic accessory function support
  - TDM support on all AIFs
  - 8 channel input and output on AIF1
- Flexible clocking, derived from MCLKn, BCLKn or SLIMbus
- 2 low-power FLLs support reference clocks down to 32kHz
- Advanced accessory detection functions
  - Low-power standby mode and configurable wake-up
- Configurable functions on 5 GPIO pins
- Integrated LDO regulators and charge pumps
- Support for single 1.8V supply operation
- Small W-CSP package, 0.4mm pitch

APPLICATIONS

- Smartphones and Multimedia handsets
- Tablets and Mobile Internet Devices (MID)
- General-purpose low-power audio CODEC hub

[1] This product is protected by Patents US 7,622,984, US 7,626,445, US 7,765,019 and GB 2,432,765

BLOCK DIAGRAM



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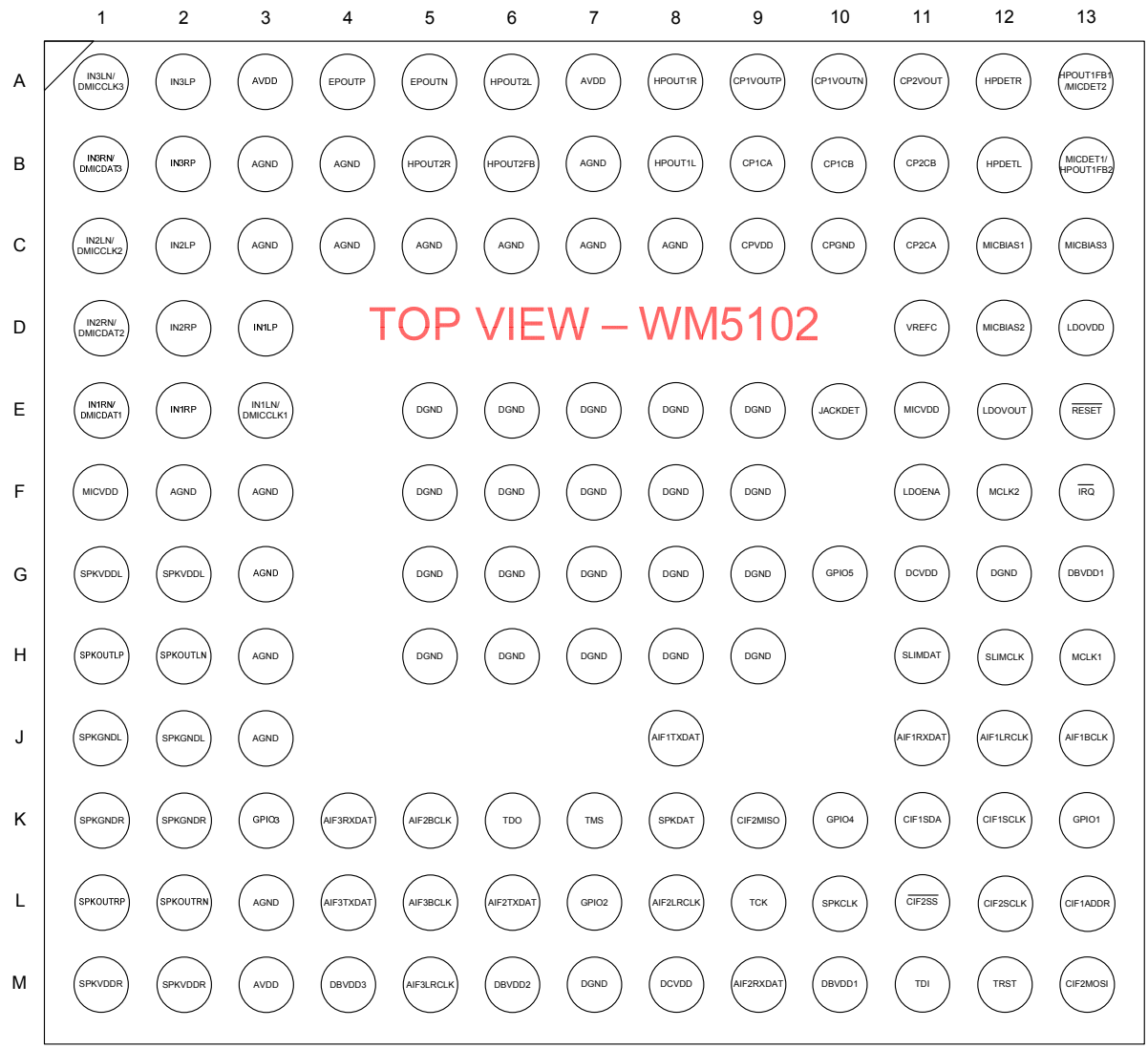
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM5102ECS/R	-40°C to +85°C	W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 5000

PIN DESCRIPTION

A description of each pin on the WM5102 is provided below.
Note that, where multiple pins share a common name, these pins should be tied together on the PCB.
All Digital Output pins are CMOS outputs, unless otherwise stated.

PIN NO	NAME	TYPE	DESCRIPTION
B3, B4, B7, C3, C4, C5, C6, C7, C8, F2, F3, G3, H3, J3, L3	AGND	Supply	Analogue ground (Return path for AVDD)
J13	AIF1BCLK	Digital Input / Output	Audio interface 1 bit clock
J11	AIF1RXDAT	Digital Input	Audio interface 1 RX digital audio data
J12	AIF1LRCLK	Digital Input / Output	Audio interface 1 left / right clock
J8	AIF1TXDAT	Digital Output	Audio interface 1 TX digital audio data
K5	AIF2BCLK	Digital Input / Output	Audio interface 2 bit clock
M9	AIF2RXDAT	Digital Input	Audio interface 2 RX digital audio data
L8	AIF2LRCLK	Digital Input / Output	Audio interface 2 left / right clock
L6	AIF2TXDAT	Digital Output	Audio interface 2 TX digital audio data
L5	AIF3BCLK	Digital Input / Output	Audio interface 3 bit clock
K4	AIF3RXDAT	Digital Input	Audio interface 3 RX digital audio data
M5	AIF3LRCLK	Digital Input / Output	Audio interface 3 left / right clock
L4	AIF3TXDAT	Digital Output	Audio interface 3 TX digital audio data
A3, A7, M3	AVDD	Supply	Analogue supply
L11	$\overline{\text{CIF2SS}}$	Digital Input	Control interface 2 Slave Select (SS)
L12	CIF2SCLK	Digital Input	Control interface 2 clock input
M13	CIF2MOSI	Digital Input	Control interface 2 Master Out / Slave In data
K9	CIF2MISO	Digital Output	Control interface 2 Master In / Slave Out data
L13	CIF1ADDR	Digital Input	Control interface 1 (I2C) address select
K12	CIF1SCLK	Digital Input	Control interface 1 clock input
K11	CIF1SDA	Digital Input / Output	Control interface 1 data input and output / acknowledge output. The output function is implemented as an Open Drain circuit.
B9	CP1CA	Analogue Output	Charge pump 1 fly-back capacitor pin
B10	CP1CB	Analogue Output	Charge pump 1 fly-back capacitor pin
A10	CP1VOUTN	Analogue Output	Charge pump 1 negative output decoupling pin
A9	CP1VOUTP	Analogue Output	Charge pump 1 positive output decoupling pin
C11	CP2CA	Analogue Output	Charge pump 2 fly-back capacitor pin
B11	CP2CB	Analogue Output	Charge pump 2 fly-back capacitor pin
A11	CP2VOUT	Analogue Output	Charge pump 2 output decoupling pin / Supply for LDO2
C10	CPGND	Supply	Charge pump 1 & 2 ground (Return path for CPVDD)
C9	CPVDD	Supply	Supply for Charge Pump 1 & 2
G13, M10	DBVDD1	Supply	Digital buffer (I/O) supply (core functions and Audio Interface 1)
M6	DBVDD2	Supply	Digital buffer (I/O) supply (for Audio Interface 2)
M4	DBVDD3	Supply	Digital buffer (I/O) supply (for Audio Interface 3)
G11, M8	DCVDD	Supply	Digital core supply
E5, E6, E7, E8, E9, F5, F6, F7, F8, F9, G5, G6, G7, G8, G9, G12, H5, H6, H7, H8, H9, M7	DGND	Supply	Digital ground (Return path for DCVDD, DBVDD1, DBVDD2 and DBVDD3)
A4	EPOUTP	Analogue Output	Earpiece positive output
A5	EPOUTN	Analogue Output	Earpiece negative output

PIN NO	NAME	TYPE	DESCRIPTION
K13	GPIO1	Digital Input / Output	General Purpose pin GPIO1. The output function is implemented as an Open Drain circuit.
L7	GPIO2	Digital Input / Output	General Purpose pin GPIO2. The output function is implemented as an Open Drain circuit.
K3	GPIO3	Digital Input / Output	General Purpose pin GPIO3. The output function is implemented as an Open Drain circuit.
K10	GPIO4	Digital Input / Output	General Purpose pin GPIO4. The output function is implemented as an Open Drain circuit.
G10	GPIO5	Digital Input / Output	General Purpose pin GPIO5. The output function is implemented as an Open Drain circuit.
B12	HPDETL	Analogue Input	Headphone left (HPOUT1L) sense input
A12	HPDETR	Analogue Input	Headphone right (HPOUT1R) sense input
A13	HPOUT1FB1/ MICDET2	Analogue Input	HPOUT1L and HPOUT1R ground feedback pin 1/ Microphone & accessory sense input 2
B8	HPOUT1L	Analogue Output	Left headphone 1 output
A8	HPOUT1R	Analogue Output	Right headphone 1 output
B6	HPOUT2FB	Analogue Input	HPOUT2L and HPOUT2R ground loop noise rejection feedback
A6	HPOUT2L	Analogue Output	Left headphone 2 output
B5	HPOUT2R	Analogue Output	Right headphone 2 output
E3	IN1LN/ DMICCLK1	Analogue Input / Digital Output	Left channel negative differential MIC input / Digital MIC clock output 1
D3	IN1LP	Analogue Input	Left channel single-ended MIC input / Left channel line input / Left channel positive differential MIC input
E1	IN1RN/ DMICDAT1	Analogue input / Digital Input	Right channel negative differential MIC input / Digital MIC data input 1
E2	IN1RP	Analogue Input	Right channel single-ended MIC input / Right channel line input / Right channel positive differential MIC input
C1	IN2LN/ DMICCLK2	Analogue Input / Digital Output	Left channel negative differential MIC input / Digital MIC clock output 2
C2	IN2LP	Analogue Input	Left channel single-ended MIC input / Left channel line input / Left channel positive differential MIC input
D1	IN2RN/ DMICDAT2	Analogue input / Digital Input	Right channel negative differential MIC input / Digital MIC data input 2
D2	IN2RP	Analogue Input	Right channel single-ended MIC input / Right channel line input / Right channel positive differential MIC input
A1	IN3LN/ DMICCLK3	Analogue Input / Digital Output	Left channel negative differential MIC input / Digital MIC clock output 3
A2	IN3LP	Analogue Input	Left channel single-ended MIC input / Left channel line input / Left channel positive differential MIC input
B1	IN3RN/ DMICDAT3	Analogue input / Digital Input	Right channel negative differential MIC input / Digital MIC data input 3
B2	IN3RP	Analogue Input	Right channel single-ended MIC input / Right channel line input / Right channel positive differential MIC input
F13	$\overline{\text{IRQ}}$	Digital Output	Interrupt Request (IRQ) output (default is active low). The pin configuration is selectable CMOS or Open Drain.
E10	JACKDET	Analogue Input	Jack detect input
F11	LDOENA	Digital Input	Enable pin for LDO1
D13	LDOVDD	Supply	Supply for LDO1

PIN NO	NAME	TYPE	DESCRIPTION
E12	LDOVOUT	Analogue Output	LDO1 output
H13	MCLK1	Digital Input	Master clock 1
F12	MCLK2	Digital Input	Master clock 2
C12	MICBIAS1	Analogue Output	Microphone bias 1
D12	MICBIAS2	Analogue Output	Microphone bias 2
C13	MICBIAS3	Analogue Output	Microphone bias 3
B13	MICDET1/ HPOUT1FB2	Analogue Input	Microphone & accessory sense input 1/ HPOUT1L and HPOUT1R ground feedback pin 2
E11, F1	MICVDD	Analogue Output	LDO2 output decoupling pin (generated internally by WM5102). (Can also be used as reference/supply for external microphones.)
E13	$\overline{\text{RESET}}$	Digital Input	Digital Reset input (active low)
H12	SLIMCLK	Digital Input / Output	SLIM Bus Clock input / output
H11	SLIMDAT	Digital Input / Output	SLIM Bus Data input / output
L10	SPKCLK	Digital Output	Digital speaker (PDM) clock output
K8	SPKDAT	Digital Output	Digital speaker (PDM) data output
J1, J2	SPKGNDL	Supply	Left speaker driver ground (Return path for SPKVDDL)
K1, K2	SPKGNDR	Supply	Right speaker driver ground (Return path for SPKVDDR)
H2	SPKOUTLN	Analogue Output	Left speaker negative output
H1	SPKOUTLP	Analogue Output	Left speaker positive output
L2	SPKOUTRN	Analogue Output	Right speaker negative output
L1	SPKOUTRP	Analogue Output	Right speaker positive output
G1, G2	SPKVDDL	Supply	Left speaker driver supply
M1, M2	SPKVDDR	Supply	Right speaker driver supply
L9	TCK	Digital Input	JTAG clock input. Internal pull-down holds this pin at logic 0 for normal operation.
M11	TDI	Digital Input	JTAG data input. Internal pull-down holds this pin at logic 0 for normal operation.
K6	TDO	Digital Output	JTAG data output
K7	TMS	Digital Input	JTAG mode select input. Internal pull-down holds this pin at logic 0 for normal operation.
M12	TRST	Digital Input	JTAG Test Access Port reset (active low). Internal pull-down holds this pin at logic 0 for normal operation.
D11	VREFC	Analogue Output	Bandgap reference decoupling capacitor connection

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (DBVDD1, LDOVDD, AVDD, DCVDD, CPVDD)	-0.3V	+2.0V
Supply voltages (DBVDD2, DBVDD3, MICVDD)	-0.3V	+4.0V
Supply voltages (SPKVDDL, SPKVDDR)	-0.3V	+6.0V
Voltage range digital inputs (DBVDD1 domain)	AGND - 0.3V	DBVDD1 + 0.3V
Voltage range digital inputs (DBVDD2 domain)	AGND - 0.3V	DBVDD2 + 0.3V
Voltage range digital inputs (DBVDD3 domain)	AGND - 0.3V	DBVDD3 + 0.3V
Voltage range digital inputs (DMICDATn)	AGND - 3.3V	MICVDD + 0.3V
Voltage range analogue inputs (INnLN)	AGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (INnLP, INnRN, INnRP)	AGND - 3.3V	MICVDD + 0.3V
Ground (DGND, CPGND, SPKGNDL, SPKGNDR)	AGND - 0.3V	AGND + 0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Operating junction temperature, T_J	-40ºC	+125ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See notes 3, 5, 6	DCVDD (≤24.576MHz clocking)	1.14	1.2	1.9	V
	DCVDD (>24.576MHz clocking)	1.71	1.8	1.9	
Digital supply range (I/O)	DBVDD1	1.7		1.9	V
Digital supply range (I/O)	DBVDD2, DBVDD3	1.7		3.47	V
LDO supply range	LDOVDD	1.7	1.8	1.9	V
Charge Pump supply range	CPVDD	1.7	1.8	1.9	V
Speaker supply range	SPKVDDL, SPKVDDR	2.4		5.5	V
Analogue supply range	AVDD	1.7	1.8	1.9	V
Microphone Bias supply See note 7	MICVDD	2.375	2.5	3.6	V
Ground	DGND, AGND, CPGND, SPKGNDL, SPKGNDR		0		V
Power supply rise time See notes 8, 9, 10	All supplies	1			µs
Operating temperature range	T_A	-40		85	°C

Notes:

1. The grounds must always be within 0.3V of AGND.
2. AVDD must be supplied before or simultaneously to DCVDD. DCVDD must not be powered if AVDD is not present. There are no other power sequencing requirements.
3. An internal LDO (powered by LDOVDD) can be used to provide the DCVDD supply.
4. The $\overline{\text{RESET}}$ input must be asserted (logic 0) during power-up, and held asserted until after the AVDD, DBVDD1 and DCVDD supplies are within the recommended operating limits. If DCVDD is powered from the internal LDO, then the $\overline{\text{RESET}}$ pin must be held asserted until at least 1.5ms after the LDO has been enabled.
5. 'Sleep' mode is supported when DCVDD is below the limits noted, provided AVDD and DBVDD1 are present.
6. Under default conditions, digital core clocking rates above 24.576MHz are inhibited. The register-controlled clocking limit should only be raised when the applicable DCVDD voltage is present.
7. An internal Charge Pump and LDO (powered by CPVDD) provide the Microphone Bias supply; the MICVDD pin should not be connected to an external supply.
8. DCVDD and MICVDD minimum rise times do not apply when these domains are powered using the internal LDOs.
9. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Wolfson strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed.
10. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 1.8V,

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Signal Level (IN1L, IN1R, IN2L, IN2R, IN3L, IN3R)						
Full-scale input signal level (0dBFS output)	V_{INFS}	Single-ended PGA input, 6dB PGA gain	0.5 -6			V_{RMS} dBV
		Differential PGA input, 0dB PGA gain	1 0			V_{RMS} dBV

Notes:

1. The full-scale input signal level is also the maximum analogue input level, before clipping occurs.
2. The full-scale input signal level changes in proportion with AVDD. For differential input, it is calculated as AVDD / 1.8.
3. A $1.0V_{RMS}$ differential signal equates to $0.5V_{RMS}$/-6dBV per input.
4. A sinusoidal input signal is assumed.

Test Conditions

T_A = +25°C

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Pin Characteristics (IN1L, IN1R, IN2L, IN2R, IN3L, IN3R)						
Input resistance	R_{IN}	Differential input, All PGA gain settings		24		kΩ
		Single-ended input, 0dB PGA gain		16		
Input capacitance	C_{IN}				5	pF

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Programmable Gain Amplifiers (PGAs)						
Minimum programmable gain				0		dB
Maximum programmable gain				31		dB
Programmable gain step size		Guaranteed monotonic		1		dB

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone Input Signal Level (DMICDAT1, DMICDAT2, DMICDAT3)						
Full-scale input signal level (0dBFS output)		0dB gain		-6		dBFS

Notes:

5. The digital microphone input signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping. Note that, because the definition of FSR is based on a sine wave, the PDM data format can support signals larger than 0dBFS.

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTnL, HPOUTnR)						
Load resistance		Normal Mode	15			Ω
		Mono Mode (BTL)	30			
		Device survival with load applied indefinitely	0.1			
Load capacitance		Direct connection, Normal Mode			400	pF
		Direct connection, Mono Mode (BTL)			200	
		Connection via 16Ω series resistor			2	nF
DC offset at Load		Single-ended mode		0.1		mV
		Differential (BTL) mode		0.2		
Earpiece Output Driver (EPOUTP+EPOUTN)						
Load resistance		Normal operation	15			Ω
		Device survival with load applied indefinitely	0.1			
Load capacitance		Direct connection (BTL)			200	pF
		Connection via 16Ω series resistor			2	nF
DC offset at Load				0.2		mV
Speaker Output Driver (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN)						
Load resistance			3			Ω
Load capacitance					200	pF
DC offset at Load				5		mV
SPKVDD leakage current				1		µA

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Paths (INnL, INnR) to ADC (Differential Input Mode, INn_MODE = 00)						
Signal to Noise Ratio (A-weighted)	SNR	High performance mode (INn_OSR = 1)	85	95		dB
		Normal mode (INn_OSR = 0)		93		
Total Harmonic Distortion	THD	-1dBV input		-88		dB
Total Harmonic Distortion Plus Noise	THD+N	-1dBV input		-86	-76	dB
Channel separation (Left/Right)				100		dB
Input noise floor		A-weighted, PGA gain = +18dB		3.2		μV_{RMS}
Common mode rejection ratio	CMRR	PGA gain = +30dB		65		dB
		PGA gain = 0dB		70		
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV(peak-peak) 10kHz		65		
Analogue Input Paths (INnL, INnR) to ADC (Single-Ended Input Mode, INn_MODE = 01) PGA Gain = +6dB unless otherwise stated.						
Signal to Noise Ratio (A-weighted)	SNR	High performance mode (INn_OSR = 1)		94		dB
		Normal mode (INn_OSR = 0)		90		
Total Harmonic Distortion	THD	-7dBV input		-81		dB
Total Harmonic Distortion Plus Noise	THD+N	-7dBV input		-80		dB
Channel separation (Left/Right)				100		dB
Input noise floor		A-weighted, PGA gain = +18dB		3.2		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		60		dB
		100mV(peak-peak) 10kHz		55		
DAC to Headphone Output (HPOUT1L, HPOUT1R; R_L = 32Ω)						
Maximum output power	P_O	0.1% THD+N		29		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms		112		dB
Total Harmonic Distortion	THD	P_O = 20mW		-86		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 20mW		-84		dB
Total Harmonic Distortion	THD	P_O = 5mW		-89		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-85		dB
Channel separation (Left/Right)		P_O = 20mW		75		dB
Output noise floor		A-weighted		2.5		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		57		dB
		100mV (peak-peak) 10kHz		57		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Headphone Output (HPOUT1L, HPOUT1R; R_L = 16Ω)						
Maximum output power	P_O	0.1% THD+N		34		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms	102	112		dB
Total Harmonic Distortion	THD	P_O = 20mW		-78		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 20mW		-76		dB
Total Harmonic Distortion	THD	P_O = 5mW		-78		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-77	-67	dB
Channel separation (Left/Right)		P_O = 20mW		75		dB
Output noise floor		A-weighted		2.5	8	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		57		dB
		100mV (peak-peak) 10kHz		57		
DAC to Line Output (HPOUT1L, HPOUT1R; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input	1 0			Vrms dBV
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms	101	110		dB
Total Harmonic Distortion	THD	0dBFS input		-83		dB
Total Harmonic Distortion Plus Noise	THD+N	0dBFS input		-81	-71	dB
Channel separation (Left/Right)				100		dB
Output noise floor		A-weighted		2.8	8	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		57		dB
		100mV (peak-peak) 10kHz		57		
DAC to Earpiece Output (HPOUT1L, HPOUT1R, Mono Mode, R_L = 32Ω BTL)						
Maximum output power	P_O	0.1% THD+N		89		mW
		5% THD+N		104		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2Vrms		113		dB
Total Harmonic Distortion	THD	P_O = 50mW		-92		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 50mW		-90		dB
Total Harmonic Distortion	THD	P_O = 5mW		-86		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-88		dB
Output noise floor		A-weighted		2.5		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		57		dB
		100mV (peak-peak) 10kHz		57		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Headphone Output (HPOUT2L, HPOUT2R; R_L = 32Ω)						
Maximum output power	P_O	0.1% THD+N		27		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms		109		dB
Total Harmonic Distortion	THD	P_O = 20mW		-90		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 20mW		-88		dB
Total Harmonic Distortion	THD	P_O = 5mW		-90		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-88		dB
Channel separation (Left/Right)		P_O = 20mW		75		dB
Output noise floor		A-weighted		3		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		57		dB
		100mV (peak-peak) 10kHz		57		
DAC to Headphone Output (HPOUT2L, HPOUT2R; R_L = 16Ω)						
Maximum output power	P_O	0.1% THD+N		32		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms	101	111		dB
Total Harmonic Distortion	THD	P_O = 20mW		-88		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 20mW		-87		dB
Total Harmonic Distortion	THD	P_O = 5mW		-85		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-83	-73	dB
Channel separation (Left/Right)		P_O = 20mW		75		dB
Output noise floor		A-weighted		2.8	10	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		57		dB
		100mV (peak-peak) 10kHz		57		
DAC to Line Output (HPOUT2L, HPOUT2R; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input	1 0			Vrms dBV
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms	100	110		dB
Total Harmonic Distortion	THD	0dBFS input		-87		dB
Total Harmonic Distortion Plus Noise	THD+N	0dBFS input		-85	-75	dB
Channel separation (Left/Right)				105		dB
Output noise floor		A-weighted		3.5	10	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		57		dB
		100mV (peak-peak) 10kHz		57		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Earpiece Output (HPOUT2L, HPOUT2R, Mono Mode, R_L = 32Ω BTL)						
Maximum output power	P_O	0.1% THD+N		85		mW
		5% THD+N		100		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2Vrms		112		dB
Total Harmonic Distortion	THD	P_O = 50mW		-90		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 50mW		-88		dB
Total Harmonic Distortion	THD	P_O = 5mW		-90		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-88		dB
Output noise floor		A-weighted		6		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		57		dB
		100mV (peak-peak) 10kHz		57		
DAC to Earpiece Output (EPOUTP+EPOUTN, R_L = 32Ω BTL)						
Maximum output power	P_O	0.1% THD+N		80		mW
		5% THD+N		100		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2Vrms	99	109		dB
Total Harmonic Distortion	THD	P_O = 50mW		-86		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 50mW		-84		dB
Total Harmonic Distortion	THD	P_O = 5mW		-85		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-83	-73	dB
Output noise floor		A-weighted		3.5	10.5	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		52		dB
		100mV (peak-peak) 10kHz		52		
DAC to Earpiece Output (EPOUTP+EPOUTN, R_L = 16Ω BTL)						
Maximum output power	P_O	0.1% THD+N		80		mW
		10% THD+N		105		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2Vrms		111		dB
Total Harmonic Distortion	THD	P_O = 50mW		-92		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 50mW		-90		dB
Total Harmonic Distortion	THD	P_O = 5mW		-84		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-82		dB
Output noise floor		A-weighted		3		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		52		dB
		100mV (peak-peak) 10kHz		52		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 8Ω, 22µH, BTL) High Performance mode (OUT4_OSR=1)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		1.4		W
		SPKVDD = 4.2V, 1% THD+N		1.0		
		SPKVDD = 3.6V, 1% THD+N		0.7		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 3.3Vrms	82	97		dB
Total Harmonic Distortion	THD	P_O = 0.9W		-70		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 0.9W		-68		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-70		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 0.5W		-68	-57	dB
Channel separation (Left/Right)		P_O = 0.5W		105		dB
Output noise floor		A-weighted		55	300	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		60		dB
		100mV (peak-peak) 10kHz		60		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV (peak-peak) 10kHz		70		
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 4Ω, 15µH, BTL) High Performance mode (OUT4_OSR=1)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		2.5		W
		SPKVDD = 4.2V, 1% THD+N		1.8		
		SPKVDD = 3.6V, 1% THD+N		1.3		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 3.3Vrms		95		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-64		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 1.0W		-62		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-66		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 0.5W		-64		dB
Channel separation (Left/Right)		P_O = 0.5W		105		dB
Output noise floor		A-weighted		55		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		60		dB
		100mV (peak-peak) 10kHz		60		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV (peak-peak) 10kHz		70		

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output (except DMICDATn and DMICCLKn) **Digital I/O is referenced to DBVDD1, DBVDD2 or DBVDD3.** **See "Recommended Operating Conditions" for the valid operating voltage range of each DBVDDn domain.**						
Input HIGH Level	V_{IH}	V_{DBVDDn} =1.8V ±10%	0.65 × V_{DBVDDn}			V
		V_{DBVDDn} =3.3V ±10%	0.7 × V_{DBVDDn}			
Input LOW Level	V_{IL}	V_{DBVDDn} =1.8V ±10%			0.35 × V_{DBVDDn}	V
		V_{DBVDDn} =3.3V ±10%			0.3 × V_{DBVDDn}	
Note that digital input pins should not be left unconnected or floating.						
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.9 × V_{DBVDDn}			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1 × V_{DBVDDn}	V
Input capacitance				10		pF
Input leakage			-1		1	µA
Pull-up resistance (where applicable)			42	49	56	kΩ
Pull-down resistance (where applicable)			80	105	130	kΩ
Digital Microphone Input / Output (DMICDATn and DMICCLKn) **DMICDATn and DMICCLKn are each referenced to a selectable supply, V_{SUP}, according to the INn_DMIC_SUP registers**						
DMICDATn input HIGH Level	V_{IH}		0.65 × V_{SUP}			V
DMICDATn input LOW Level	V_{IL}				0.35 × V_{SUP}	V
DMICCLKn output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 × V_{SUP}			V
DMICCLKn output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 × V_{SUP}	V
Input capacitance				10		pF
Input leakage			-1		1	µA
SLIMbus Digital Input / Output (SLIMCLK and SLIMDAT) **1.8V I/O Signalling (ie. 1.65V ≤ DBVDD1 ≤1.95V)**						
Input HIGH Level	V_{IH}		0.65 × V_{DBVDD1}			V
Input LOW Level	V_{IL}				0.35 × V_{DBVDD1}	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.9 × V_{DBVDD1}			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1 × V_{DBVDD1}	V
Pin capacitance					5	pF
General Purpose Input / Output (GPIOn)						
Clock output frequency		GPIO pin configured as OPCLK or FLL output			26.5	MHz

Test Conditions

fs ≤ 48kHz

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Decimation Filters						
Passband		+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
Passband ripple					+/- 0.05	dB
Stopband			0.546 fs			
Stopband attenuation		f > 0.546 fs	85			dB
Signal path delay		Analogue input to Digital AIF output			2	ms
DAC Interpolation Filters						
Passband		+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
Passband ripple					+/- 0.05	dB
Stopband			0.546 fs			
Stopband attenuation		f > 0.546 fs	85			dB
Signal path delay		Digital AIF input to Analogue output			1.5	ms

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias (MICBIAS1, MICBIAS2, MICBIAS3)						
Note - No capacitor on MICBIASn						
Note - In regulator mode, it is required that V_{MICVDD} - $V_{MICBIASn}$ > 200mV						
Minimum Bias Voltage	$V_{MICBIAS}$	Regulator mode (MICBn_BYPASS=0) Load current ≤ 1.0mA		1.5		V
Maximum Bias Voltage				2.8		V
Bias Voltage output step size				0.1		V
Bias Voltage accuracy			-5%		+5%	V
Bias Current		Regulator mode (MICBn_BYPASS=0), V_{MICVDD} - $V_{MICBIAS}$ >200mV			2.4	mA
		Bypass mode (MICBn_BYPASS=1)			5.0	
Output Noise Density		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, Measured at 1kHz		50		nV/√Hz
Integrated noise voltage		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, 100Hz to 7kHz, A-weighted		4		µVrms
Power Supply Rejection Ratio (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		95		dB
		100mV (peak-peak) 10kHz		65		
Load capacitance		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=0			50	pF
		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=1	1.8	4.7		µF
Output discharge resistance		MICBn_ENA=0, MICBn_DISCH=1		5		kΩ
External Accessory Detect						
Load impedance detection range (HPDETL or HPDETR)		HP_IMPEDANCE_ RANGE=00	4		80	Ω
		HP_IMPEDANCE_ RANGE=01	70		1000	
		HP_IMPEDANCE_ RANGE=10	1000		10000	
Load impedance detection accuracy (HPDETL or HPDETR)			-30		+30	%
Load impedance detection range (MICDET1 or MICDET2) 2.2kΩ (2%) MICBIAS resistor. Note these characteristics assume no other component is connected to MICDETn.		for MICD_LVL[0] = 1	0		3	Ω
		for MICD_LVL[1] = 1	17		21	
		for MICD_LVL[2] = 1	36		44	
		for MICD_LVL[3] = 1	62		88	
		for MICD_LVL[4] = 1	115		160	
		for MICD_LVL[5] = 1	207		381	
		for MICD_LVL[8] = 1	475		30000	
Jack Detection input threshold voltage (JACKDET)	$V_{JACKDET}$	Jack insertion		0.5 x AVDD		V
		Jack removal		0.85 x AVDD		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICVDD Charge Pump and Regulator (CP2 and LDO2)						
Output voltage	V_{MICVDD}		1.7	2.7	3.3	V
Programmable output voltage step size				50		mV
Maximum output current				8		mA
Start-up time		4.7µF on MICVDD, $I_{MICBIASn}$ = 1mA		4.5		ms
Frequency Locked Loop (FLL1, FLL2)						
Output frequency		Normal operation, input reference supplied	13		52	MHz
		Free-running mode, no reference supplied		30		
Lock Time		F_{REF} = 32kHz, F_{OUT} = 24.576MHz		10		ms
		F_{REF} = 12MHz, F_{OUT} = 24.576MHz		1		
RESET pin Input						
RESET input pulse width (To trigger a Hardware Reset, the RESET input must be asserted for longer than this duration)			1			µs

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

Device Reset Thresholds						
AVDD Reset Threshold	V_{AVDD}		0.54		0.96	V
DCVDD Reset Threshold	V_{DCVDD}		0.59		0.81	V
DBVDD1 Reset Threshold	V_{DBVDD1}		0.54		0.96	V
Note that the reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in the “Recommended Operating Conditions” section. Refer to this section for the WM5102 power-up sequencing requirements.						

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied. (Note that this is measured without any mute function enabled.)
2. Total Harmonic Distortion (dB) – THD is the ratio of the RMS sum of the harmonic distortion products in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (ie. test frequency) output.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (ie. test frequency) output.
4. Power Supply Rejection Ratio (dB) - PSRR is the ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
5. Common Mode Rejection Ratio (dB) – CMRR is the ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
6. Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
7. Multi-Path Crosstalk (dB) – is the difference in level between the output of the active path and the measured signal level in the idle path at the test signal frequency. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
8. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
9. All performance measurements are specified with a 20kHz low pass ‘brick-wall’ filter and, where noted, an A-weighted filter. Failure to use these filters will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise.

DEVICE DESCRIPTION

INTRODUCTION

The WM5102 is a highly integrated low-power audio hub CODEC for mobile telephony and portable devices. It provides flexible, high-performance audio interfacing for handheld devices in a small and cost-effective package. It supports programmable DSP for wideband voice processing, ideally suited for multimedia phones and smartphones.

The WM5102 digital core provides an extensive capability for signal processing algorithms, including echo cancellation, wind noise, side-tone and other programmable filters. Parametric equalisation (EQ) and dynamic range control (DRC) are also supported. Highly flexible digital mixing, including stereo full-duplex asynchronous sample rate conversion, provides use-case flexibility across a broad range of system architectures. A signal generator for controlling haptics vibe actuators is included.

The WM5102 provides multiple digital audio interfaces, including SLIMbus, in order to provide independent and fully asynchronous connections to different processors (eg. application processor, baseband processor and wireless transceiver).

A flexible clocking arrangement supports a wide variety of external clock references, including clocking derived from the digital audio interface. Two integrated Frequency Locked Loop (FLL) circuits provide additional flexibility.

Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications. Configurable 'Wake-Up' actions can be associated with the low-power standby (Sleep) mode.

Versatile GPIO functionality is provided, and support for external accessory / push-button detection inputs. Comprehensive Interrupt (IRQ) logic and status readback are also provided.

HI-FI AUDIO CODEC

The WM5102 is a high-performance low-power audio CODEC which uses a simple analogue architecture. 6 ADCs and 7 DACs are incorporated, providing a dedicated ADC for each input and a dedicated DAC for each output channel.

The analogue outputs comprise two 29mW (113dB SNR) stereo headphone amplifiers with ground-referenced output, a 100mW differential (BTL) earpiece driver, and a Class D stereo speaker driver capable of delivering 2W per channel into a 4Ω load. Six analogue inputs are provided, each supporting single-ended or differential input modes. In differential mode, the input path SNR is 96dB. The ADC input paths can be bypassed, supporting up to 6 channels of digital microphone input.

The audio CODEC is controlled directly via register access. The simple analogue architecture, combined with the integrated tone generator, enables simple device configuration and testing, minimising debug time and reducing software effort.

The WM5102 output drivers are designed to support as many different system architectures as possible. Each output has a dedicated DAC which allows mixing, equalisation, filtering, gain and other audio processing to be configured independently for each channel. This allows each signal path to be individually tailored for the load characteristics. All outputs have integrated pop and click suppression features.

The headphone output drivers are ground-referenced, powered from an integrated charge pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. Ground loop feedback is incorporated, providing rejection of noise on the ground connections. A mono mode is available on the headphone outputs; this configures the drivers as differential (BTL) outputs, suitable for an earpiece or hearing aid coil.

The Class D speaker drivers deliver excellent power efficiency. High PSRR, low leakage and optimised supply voltage ranges enable powering from switching regulators or directly from the battery. Battery current consumption is minimised across a wide variety of voice communication and multimedia playback use cases.

The WM5102 is cost-optimised for a wide range of mobile phone applications, and features two channels of Class D power amplification. For applications requiring more than two channels of power amplification (or when using the integrated Class D path to drive a haptics actuator), the PDM output channels can be used to drive two external PDM-input speaker drivers. In applications where stereo loudspeakers are physically widely separated, the PDM outputs can ease layout and EMC by avoiding the need to run the Class-D speaker outputs over long distances and interconnects.

DIGITAL AUDIO CORE

The WM5102 uses a core architecture based on all-digital signal routing, making digital audio effects available on all signal paths, regardless of whether the source data input is analogue or digital. The digital mixing desk allows different audio effects to be applied simultaneously on many independent paths, whilst also supporting a variety of sample rates concurrently. This helps support many new audio use-cases. Soft mute and un-mute control allows smooth transitions between use-cases without interrupting existing audio streams elsewhere.

The WM5102 digital core provides an extensive capability for programmable signal processing algorithms. The DSP can support functions such as echo cancellation, wind noise, side-tone and other programmable filters. The DSP is optimised for advanced voice processing, but a wide range of application-specific filters and audio enhancements can also be implemented.

Highly flexible digital mixing, including mixing between audio interfaces, is possible. The WM5102 performs stereo full-duplex asynchronous sample rate conversion, providing use-case flexibility across a broad range of system architectures. Automatic sample rate detection is provided, enabling seamless wideband/narrowband voice call handover.

Dynamic Range Controller (DRC) functions are available for optimising audio signal levels. In playback modes, the DRC can be used to maximise loudness, while limiting the signal level to avoid distortion, clipping or battery droop, in particular for high-power output drivers such as speaker amplifiers. In record modes, the DRC assists in applications where the signal level is unpredictable.

The 5-band parametric equaliser (EQ) functions can be used to compensate for the frequency characteristics of the output transducers. EQ functions can be cascaded to provide additional frequency control. Programmable high-pass and low-pass filters are also available for general filtering applications such as removal of wind and other low-frequency noise.

DIGITAL INTERFACES

Three serial digital audio interfaces (AIFs) each support PCM, TDM and I2S data formats for compatibility with most industry-standard chipsets. AIF1 supports eight input/output channels; AIF2 and AIF3 each support two input/output channels. Bidirectional operation at sample rates up to 192kHz is supported.

Six digital PDM input channels are available (three stereo interfaces); these are typically used for digital microphones, powered from the integrated MICBIAS power supply regulators. Two PDM output channels are also available (one stereo interface); these are typically used for external power amplifiers. Embedded mute codes provide a control mechanism for external PDM-input devices.

The WM5102 features a MIPI-compliant SLIMbus interface, providing eight channels of audio input/output. Mixed audio sample rates are supported on the SLIMbus interface. The SLIMbus interface also supports read/write access to the WM5102 control registers.

The WM5102 is equipped with an I2C slave port (at up to 1MHz), and an SPI port (at up to 26MHz). Full access to the register map is also provided via the SLIMbus port.

OTHER FEATURES

The WM5102 incorporates two 1kHz tone generators which can be used for 'beep' functions through any of the audio signal paths. The phase relationship between the two generators is configurable, providing flexibility in creating differential signals, or for test scenarios.

A white noise generator is provided, which can be routed within the digital core. The noise generator can provide 'comfort noise' in cases where silence (digital mute) is not desirable.

Two Pulse Width Modulation (PWM) signal generators are incorporated. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting. The PWM signal generators can be output directly on a GPIO pin.

The WM5102 provides 5 GPIO pins, supporting selectable input/output functions for interfacing, detection of external hardware, and to provide logic outputs to other devices. Comprehensive Interrupt (IRQ) functionality is also provided for monitoring internal and external event conditions.

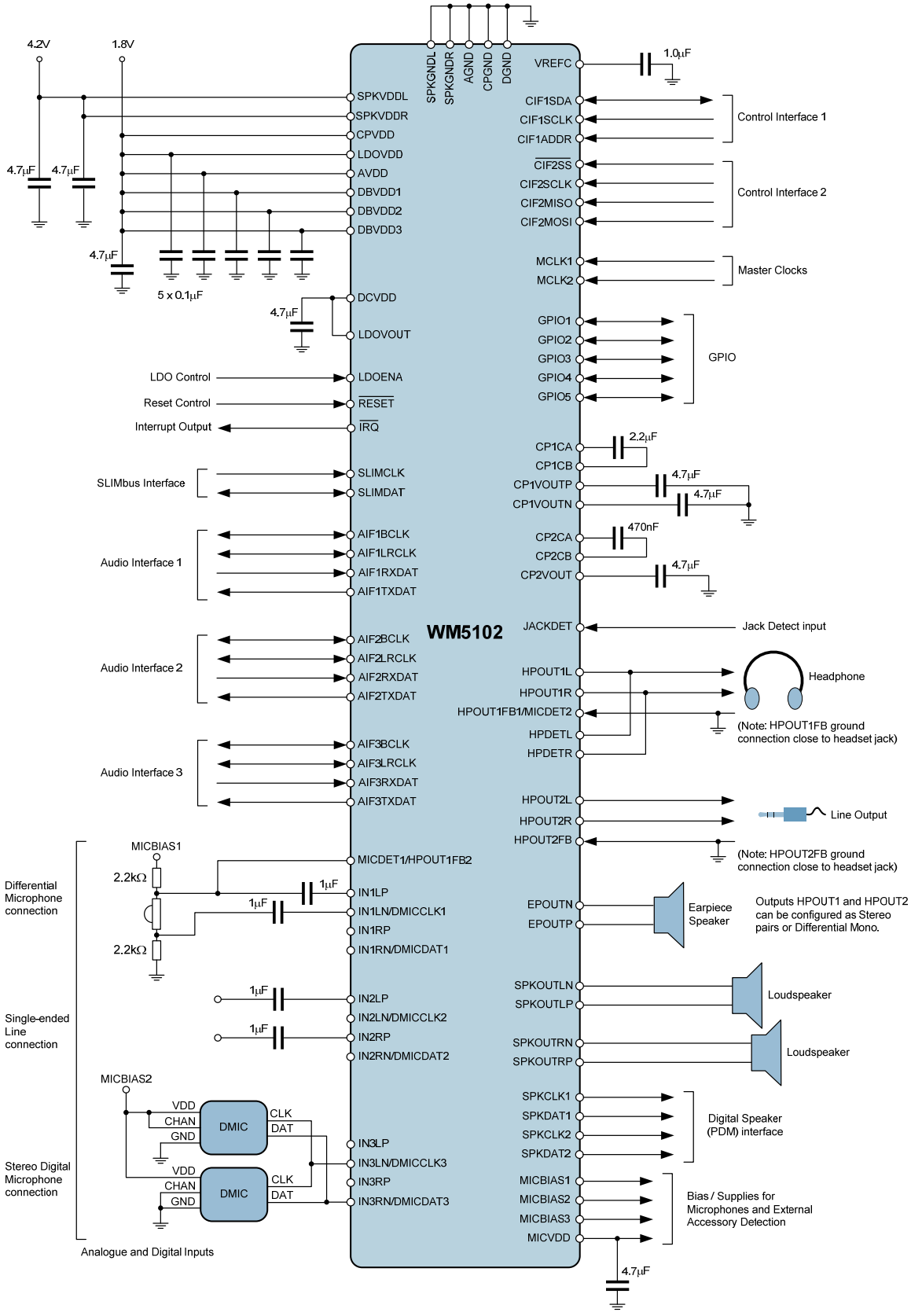
A signal generator for controlling haptics devices is included, compatible with both Eccentric Rotating Motor (ERM) and Linear Resonant Actuator (LRA) haptic devices. The haptics signal generator is highly configurable, and can execute programmable drive event profiles, including reverse drive control. An external vibe actuator can be driven directly by the Class D speaker output.

The WM5102 can be powered from a 1.8V external supply. A separate supply (4.2V) is typically required for the Class D speaker driver. Integrated Charge Pump and LDO Regulators circuits are used to generate supply rails for internal functions and to support powering or biasing of external microphones.

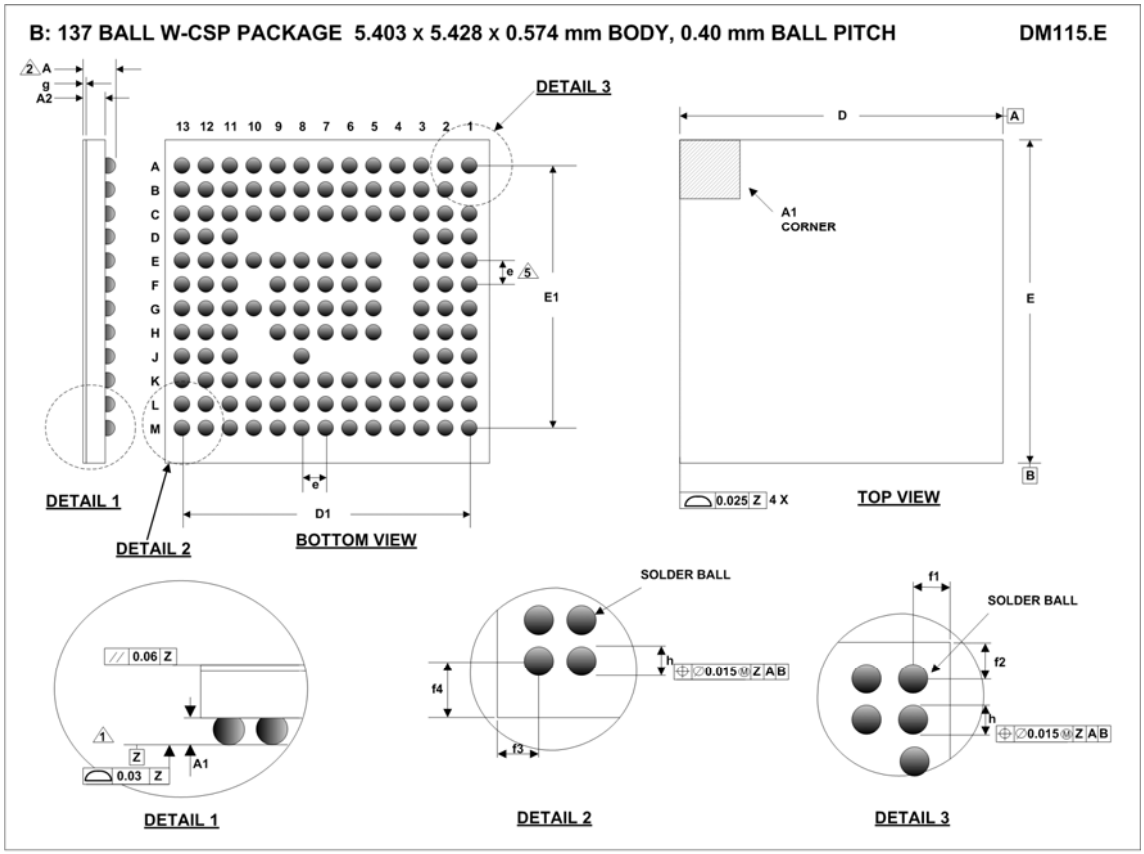
A smart accessory interface is included, supporting most standard 3.5mm accessories. Jack detection, accessory sensing and impedance measurement is provided, for external accessory and push-button detection. Accessory detection can be used as a 'Wake-Up' trigger from low-power standby. Microphone activity detection with interrupt is also available.

System clocking can be derived from the MCLK1 or MCLK2 input pins. Alternatively, the SLIMbus interface, or the audio interfaces (configured in Slave mode), can be used to provide a clock reference. Two integrated Frequency Locked Loop (FLL) circuits provide support for a wide range of clocking configurations, including the use of a 32kHz input clock reference.

RECOMMENDED EXTERNAL COMPONENTS



PACKAGE DIMENSIONS



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.540	0.574	0.608	
A1	0.172	0.202	0.232	
A2	0.356	0.372	0.388	
D	5.378	5.403	5.428	
D1		4.80 BSC		
E	5.403	5.428	5.453	
E1		4.40 BSC		
e		0.400 BSC		5
f1		0.300 BSC		
f2		0.427 BSC		
f3		0.303 BSC		
f4		0.601 BSC		
g		0.022		
h	0.222	0.262	0.302	

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

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ADDRESS:

Wolfson Microelectronics plc

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com

REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
15/09/11	1.0	Customer preview under NDA		MP
24/10/11	1.1	Updates to Control Interface, Haptics description and Pin names		MP
11/11/11	1.2	Removed DACVDD		MP
7/12/11	1.3	Updated power pins to reflect implementation, and block diagram to match. Updated filter spec delay wording		MP
17/02/12	1.4	Updates to all sections, and alignment with datasheet standards.		PH
7/03/12	1.4	Pin Configuration / Ballout details added	4-7	PH
22/03/12	1.4	Package Drawing added	27	PH
13/04/12	1.4	Reel quantity added	4	PH
19/04/12	1.5	Updates to Electrical Characteristics		KOL
01/05/12	1.6	Signal Timing Requirements deleted		PH
08/06/12	1.6	Sample rates greater than 192kHz deleted. DCVDD requirements for 50MHz clocking added. Analogue connections updated on External Components figure. Maximum LDO2 output voltage amended to 3.25V.		PH
08/08/12	1.6	Pin Descriptions updated to show single-ended analogue input is on the INxP pins (not INxN).		PH
23/10/12	2.0	Electrical Characteristics updated Package Drawing updated		PH
13/11/12	2.0	Electrical Characteristics updated. Correction to Pin Numbering (SPKOUTLP, SPKOUTLN, SPKOUTRP, SPKOUTRN)		PH
14/12/12	3.0	Block diagram update, showing gain in AEC Loopback path Package drawing updated		PH
19/02/13	3.0	Electrical Characteristics updated		PH
22/02/13	3.0	Pin Description updated.		JMacD
04/06/13	4.0	Electrical Characteristics updated		JMacD
26/02/14	4.1	Power-up timing and Reset requirements updated. SNR test conditions clarified. Headphone impedance measurement control updated. Clarification to maximum input signal levels (analogue & digital).		JMacD
27/06/14	4.2	JTAG Interface input pins all have internal pull-down resistors. Updated Pull-up/Pull-down resistances, and Reset thresholds.	7 17, 20	PH