

October 1987 Revised May 2002

MM74C165

Parallel-Load 8-Bit Shift Register

General Description

The MM74C165 functions as an 8-bit parallel-load, serial shift register. Data is loaded into the register independent of the state of the clock(s) when PARALLEL LOAD (\overline{PL}) is low. Shifting is inhibited as long as \overline{PL} is low. Data is sequentially shifted from complementary outputs, Q_7 and $\overline{Q_7}$, highest-order bit (P7) first. New serial data may be entered via the SERIAL DATA (Ds) input. Serial shifting occurs on the rising edge of CLOCK1 or CLOCK2. Clock inputs may be used separately or together for combined clocking from independent sources. Either clock input may be used also as an active-low clock enable. To prevent double-clocking when a clock input is used as an enable, the enable must be changed to a high level (disabled) only while the clock is HIGH.

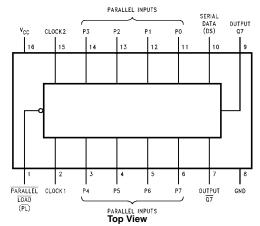
Features

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L
- Parallel loading independent of clock
- Dual clock inputs
- Fully static operation

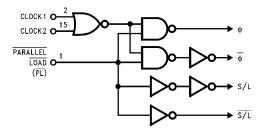
Ordering Code:

Order Number	Package Number	Package Description
	•	5 ,
MM74165N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

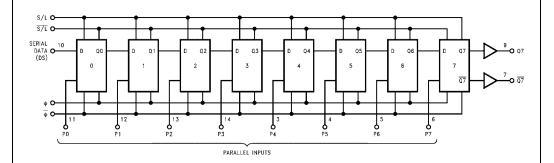
Connection Diagram



Block Diagrams



*Please look into Section 8, Appendix D for availability of various package types.



Truth Table

State	Inputs				Internal		Outputs		
	PL	Clock1	Clock2	Ds	P0 thru P7	Q0	Q1	Q7	Q7
			(as enable)						
Parallel Load	L	Х	Х	Х	P0P7	P0	P1	P7	P7
Enable	Н	L	L	Х	Х	P0	P1	P7	P7
Shift (with Ds)	Н	1	L	Н	Х	Н	P0	P6	P6
Shift (with Ds)	Н	1	L	L	Х	L	Н	P5	P5
Hold (Disable)	Н	1	Н	Х	Х	L	Н	P5	P5

X = Don't Care $H = V_{IN(1)}$

$$\begin{split} & \Pi = v_{IN(1)} \\ & = V_{IN(0)} \\ & \uparrow = Clock transition from \ V_{IN(0)} \ to \ V_{IN(1)} \\ & P0 \ thru \ P7 = Data \ present (and loaded into) \ parallel inputs \\ & Q0 \ thru \ Q6 = Internal \ flip-flop \ outputs \end{split}$$

Absolute Maximum Ratings(Note 1)

 $\begin{tabular}{lll} Voltage at Any Pin & -0.3V to $V_{\rm CC}$ + 0.3V \\ Operating Temperature Range & -55^{\circ}C to +125^{\circ}C \\ Storage Temperature Range & -65^{\circ}C to +150^{\circ}C \\ Absolute Maximum $V_{\rm CC}$ & 18V \\ \end{tabular}$

Power Dissipation

Dual-In-Line 700 mW Small Outline 500 mW

Operating V_{CC} Range 3V to 15V

Lead Temperature

(Soldering, 10 seconds) 260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions

for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS TO	CMOS				•	-
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 5V	3.5			V
		$V_{CC} = 10V$	8.0			V
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 5V			1.5	V
		V _{CC} = 10V			2.0	V
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_{O} = -10 \mu A$	4.5			V
		$V_{CC}=10V,\ I_O=-10\ \mu A$	9.0			V
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_{O} = +10 \mu A$			0.5	V
		$V_{CC} = 10V, I_{O} = +10 \mu A$			1.0	V
I _{IN(1)}	Logical "1" Input Current	V _{CC} = 15V, V _{IN} = 15V		0.005	1.0	μΑ
I _{IN(0)}	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μΑ
I _{CC}	Supply Current	V _{CC} = 15V		0.05	300	μΑ
CMOS TO	LPTTL INTERFACE					
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 4.75V	V _{CC} - 1.5			V
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 4.75V			0.8	V
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{O} = -360 \mu A$	2.4			V
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 4.75V, I_{O} = 360 \mu A$			0.4	V
OUTPUT D	RIVE (See Family Characteristics	Data Sheet) (short circuit current)				
I _{SOURCE}	Output Source Current	V _{CC} = 5V	-1.75	-3.3		mA
	(P-Channel)	$T_A = 25$ °C, $V_{OUT} = 0$ V	-1.73	-3.3		IIIA
I _{SOURCE}	Output Source Current	V _{CC} = 10V	-8.0	-15		mA
	(P-Channel)	$T_A = 25^{\circ}C$, $V_{OUT} = 0V$	-6.0			IIIA
I _{SINK}	Output Sink Current	V _{CC} = 5V	1.75	3.6		mA
	(N-Channel)	$T_A = 25$ °C, $V_{OUT} = V_{CC}$	1.75	3.0		IIIA
I _{SINK}	Output Sink Current	V _{CC} = 10V	8.0	16		mA
	(N-Channel)	$T_A = 25$ °C, $V_{OUT} = V_{CC}$	0.0	10		IIIA

AC Electrical Characteristics (Note 2)

 $T_A=25^{\circ}C,\ C_L=50$ pF, unless otherwise noted

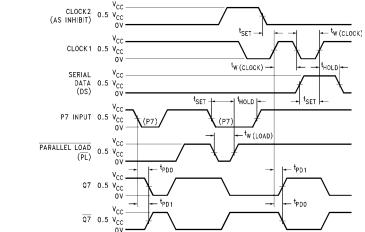
Symbol	Parameter	Conditions	Min	Тур	Max	Units	
t _{pd0} , t _{pd1}	Propagation Delay Time to a Logical "0" or	$V_{CC} = 5V$		200	400	400 ns	
	Logical "1" from Clock or Load to Q or Q	V _{CC} = 10V		80	200	113	
t _{pd0} , t _{pd1}	Propagation Delay Time to a Logical "0" or	$V_{CC} = 5V$		200	400		
	Logical "1" from H to Q or Q	V _{CC} = 10V		80	200	ns	
t _S	Clock Inhibit Set-up Time	$V_{CC} = 5V$	150	75			
		V _{CC} = 10V	60	30		ns	
t _S	Serial Input Set-up Time	V _{CC} = 5V	50	25		ns	
		V _{CC} = 10V	30	15			
t _H	Serial Input Hold Time	V _{CC} = 5V	50	0		ns	
		V _{CC} = 10V	30	0			
t _S	Parallel Input Set-Up Time	V _{CC} = 5V	150	75		ns	
		V _{CC} = 10V	60	30		115	
t _H	Parallel Input Hold Time	$V_{CC} = 5V$	50	0		ns	
		V _{CC} = 10V	30	0		ns	
t _W	Minimum Clock Pulse Width	$V_{CC} = 5V$		70	200	ns	
		V _{CC} = 10V		30	100		
t _W	Minimum Load Pulse Width	V _{CC} = 5V		85	180	ns	
		V _{CC} = 10V		30	90	113	
f _{MAX}	Maximum Clock Frequency	V _{CC} = 5V	2.5	6		MHz	
		V _{CC} = 10V	5	12		IVITIZ	
t _r , t _f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$	10			μs	
		V _{CC} = 10V	5				
C _{IN}	Input Capacitance	(Note 3)		5		pF	
C _{PD}	Power Dissipation Capacitance	(Note 4)		65		pF	

Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

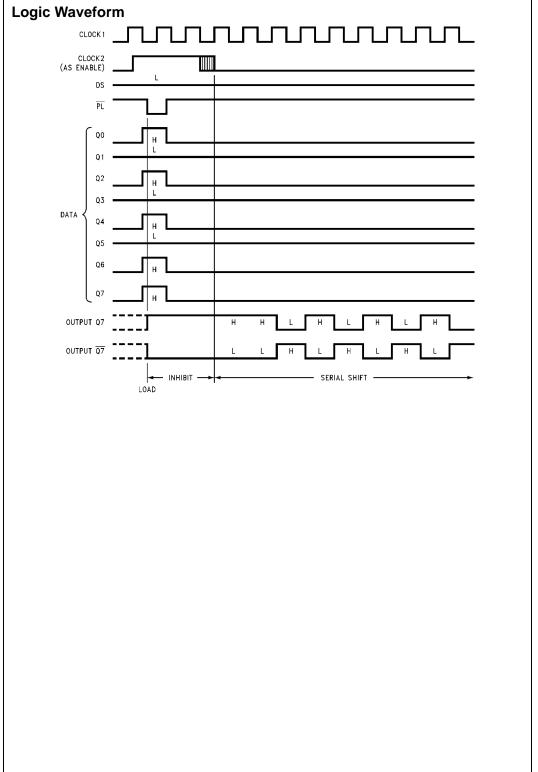
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note AN-90.

Switching Time Waveform



Note A: The remaining six data and the serial input are LOW.

Note B: Prior to test, HIGH level data is loaded into the P7 input.



Physical Dimensions inches (millimeters) unless otherwise noted 0.740 - 0.780 0.090 (18.80 - 19.81)(2.286)<u>16 15 14 13 12 11 10 9</u> 16 15 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 2 3 4 5 6 7 8 1 2 IDENT IDENT OPTION 01 OPTION 02 0.065 0.130 ± 0.005 $\frac{0.060}{(1.524)}$ 4º TYP 0.300 - 0.320 (1.651) $\overline{(3.302 \pm 0.127)}$ OPTIONAL (7.620 - 8.128) 0.145 - 0.200 (3.683 - 5.080)95°±5° $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 90° ± 4° TYP 0.020 MIN 0.280 (0.508) $\frac{0.125 - 0.150}{(3.175 - 3.810)}$ (7.112) MIN (0.762 ± 0.381) 0.014 - 0.023 0.100 ± 0.010 (0.325 +0.040 -0.015 (0.356 - 0.584) (2.540 ± 0.254) 0.050 ± 0.010 (1.270 ± 0.254) N16E (REV F) TYP

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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