



**ALPHA & OMEGA**  
SEMICONDUCTOR

**AOCA32317**

**30V Common-Drain Dual N-Channel MOSFET**

#### General Description

- Trench Power MOSFET technology
- Low  $R_{SS(ON)}$
- ESD protection
- Common drain configuration for design simplicity
- RoHS and Halogen-Free Compliant

#### Product Summary

$V_{SS}$	30V
$R_{SS(ON)}$ (at $V_{GS}=10V$ )	< 7.3mΩ
$R_{SS(ON)}$ (at $V_{GS}=4.5V$ )	< 10.2mΩ

#### Applications

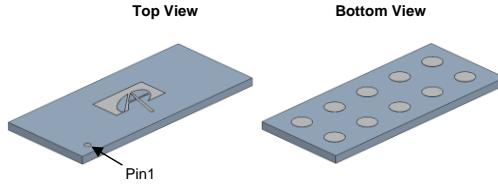
- Battery protection switch
- Type C - PD load switch

#### Typical ESD protection

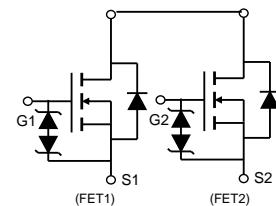
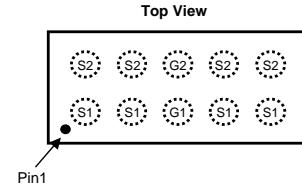
HBM Class 2



AlphaDFN™ 3.37x1.47\_10



Top View      Bottom View



#### Orderable Part Number

AOCA32317

#### Package Type

AlphaDFN™3.37x1.47\_10

#### Form

Tape & Reel

#### Minimum Order Quantity

5000

#### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Rating	Units
Source-Source Voltage	$V_{SS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Source Current(DC) <sup>Note1</sup>	$I_S$   $T_A=25^\circ\text{C}$	17	A
Source Current(Pulse) <sup>Note2</sup>	$I_{SM}$	100	
Power Dissipation <sup>Note1</sup>	$P_D$   $T_A=25^\circ\text{C}$	3.1	W
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C

#### Thermal Characteristics

Parameter	Symbol	Typical	Units
Maximum Junction-to-Ambient   $t \leq 10\text{s}$	$R_{JJA}$	30	°C/W
Maximum Junction-to-Ambient   Steady-State		40	°C/W

**Note 1.**  $I_S$  rated value is based on bare silicon. Mounted on 70mmx70mm FR-4 board.

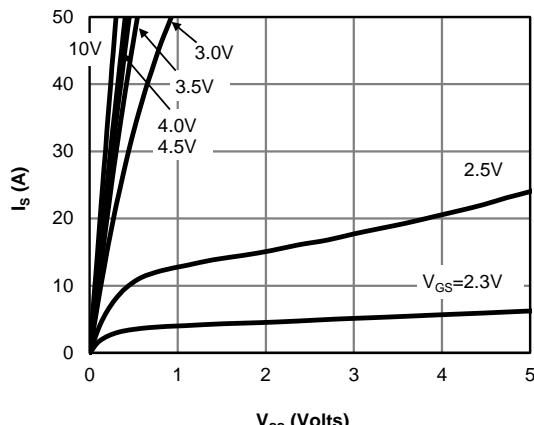
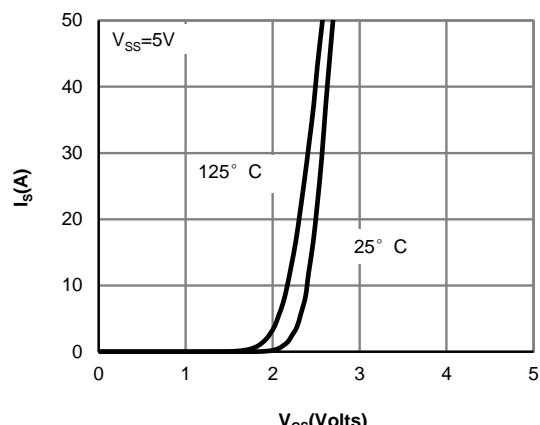
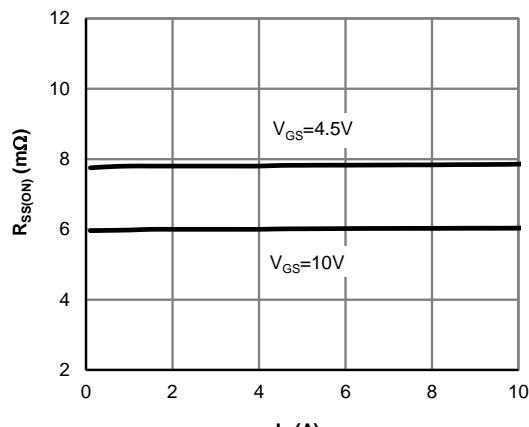
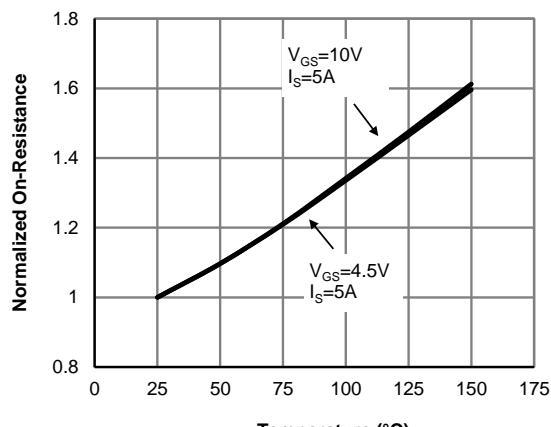
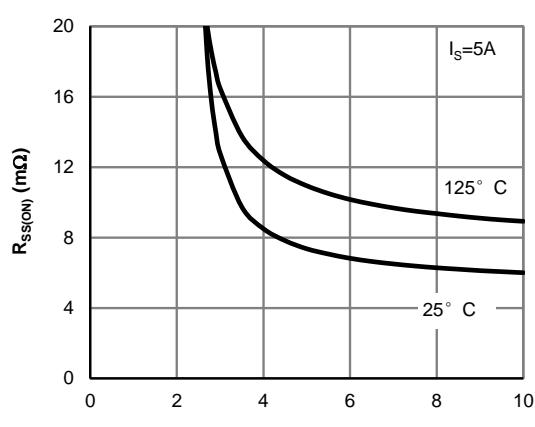
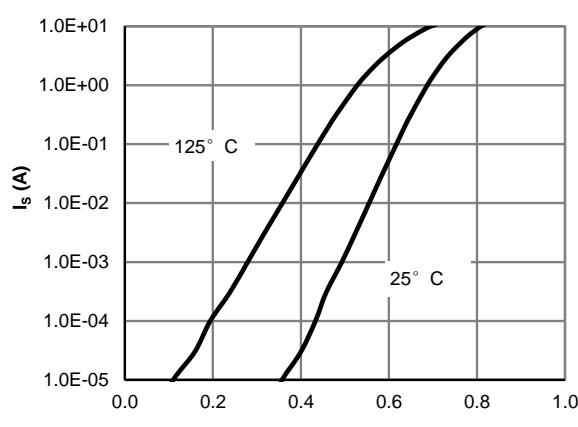
**Note 2.** PW <10  $\mu\text{s}$  pulses, duty cycle 1% max.

**Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$\text{BV}_{\text{SSS}}$	Source-Source Breakdown Voltage	$I_S=250\mu\text{A}, V_{GS}=0\text{V}$	Test Circuit 6	30		V
$I_{\text{SSS}}$	Zero Gate Voltage Source Current	$V_{SS}=30\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$	Test Circuit 1		1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate leakage current	$V_{SS}=0\text{V}, V_{GS}=\pm20\text{V}$	Test Circuit 2		5	$\mu\text{A}$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{SS}=V_{GS}, I_S=250\mu\text{A}$	Test Circuit 3	1.1	1.5	2
$R_{\text{SS(ON)}}$	Static Source to Source On-Resistance	$V_{GS}=10\text{V}, I_S=5\text{A}$	Test Circuit 4	4.2	6	7.3
		$T_J=125^\circ\text{C}$		6.3	9	11
$g_{\text{FS}}$	Forward Transconductance	$V_{SS}=5\text{V}, I_S=5\text{A}$	Test Circuit 3		37	S
$V_{\text{FSS}}$	Forward Source to Source Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$	Test Circuit 5		0.7	1
<b>DYNAMIC PARAMETERS</b>						
$R_g$	Gate resistance	$f=1\text{MHz}$			208	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g$	Total Gate Charge	$V_{G1S1}=10\text{V}, V_{SS}=15\text{V}, I_S=5\text{A}$		50	70	nC
$t_{D(\text{on})}$	Turn-On Delay Time	$V_{G1S1}=10\text{V}, V_{SS}=15\text{V}, R_L=3\Omega, R_{\text{GEN}}=3\Omega$		0.12		$\mu\text{s}$
$t_r$	Turn-On Rise Time			0.23		$\mu\text{s}$
$t_{D(\text{off})}$	Turn-Off Delay Time		Test Circuit 8	1.29		$\mu\text{s}$
$t_f$	Turn-Off Fall Time			0.78		$\mu\text{s}$

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 1: On-Region Characteristics**

**Figure 2: Transfer Characteristics**

**Figure 3: On-Resistance vs. Source Current and Gate Voltage**

**Figure 4: On-Resistance vs. Junction Temperature**

**Figure 5: On-Resistance vs. Gate-Source Voltage**

**Figure 6: Forward Source to Source Characteristics**

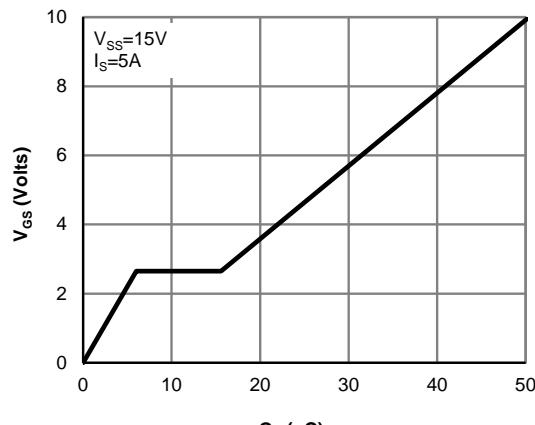
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Figure 7: Gate-Charge Characteristics

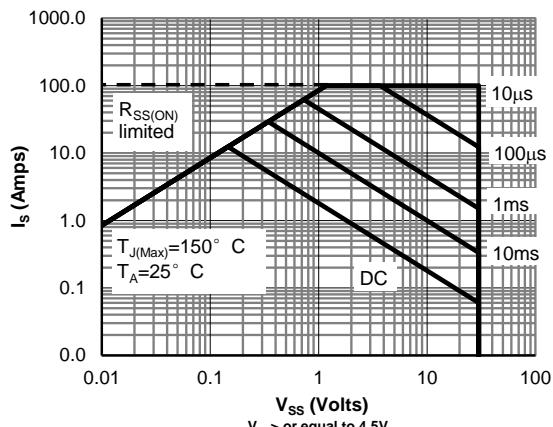
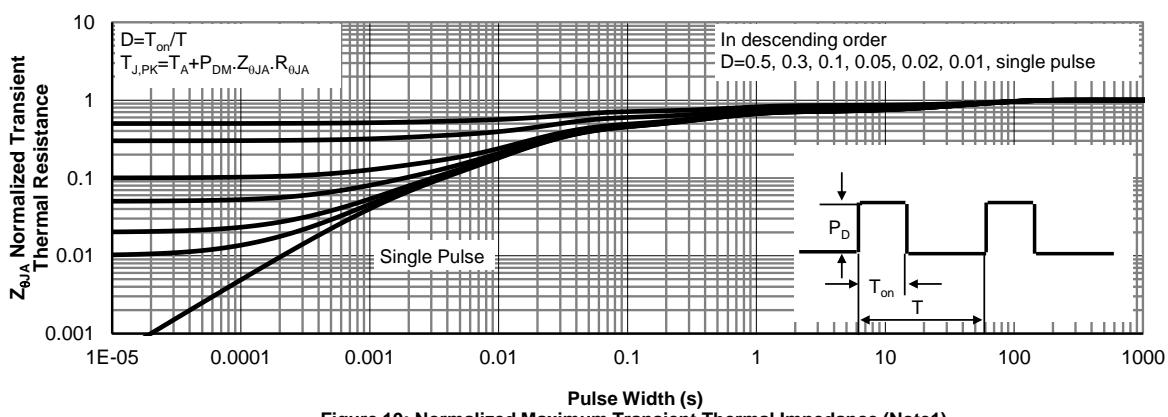
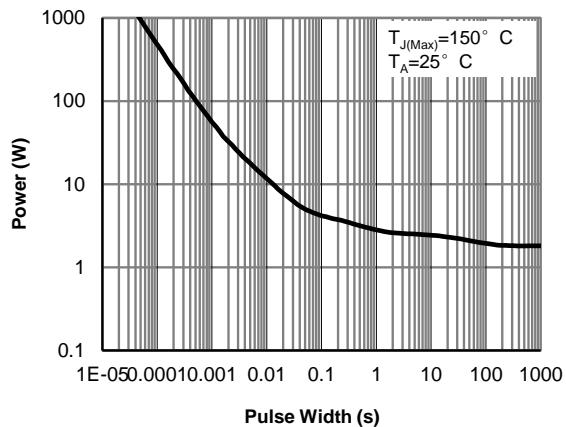
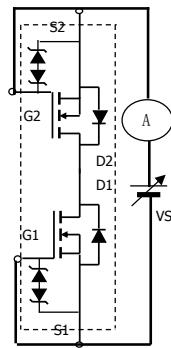
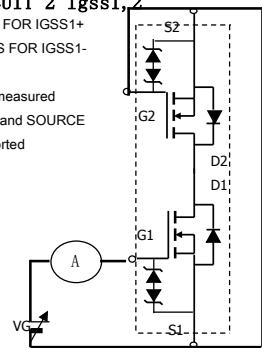
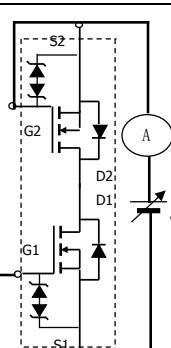
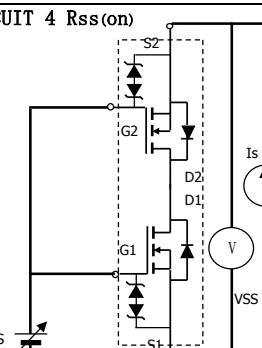
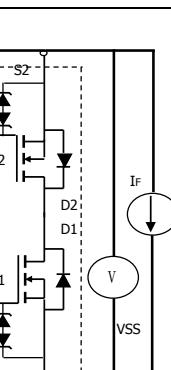
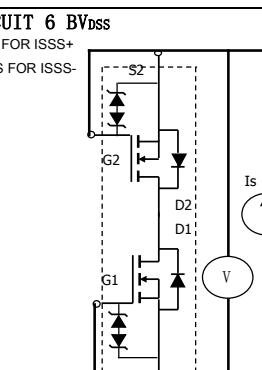
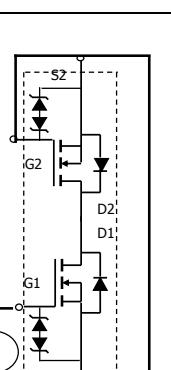


Figure 8: Maximum Forward Biased Safe Operating Area (Note1)



<b>TEST CIRCUIT 1 Isss</b> POSITIVE VSS FOR ISSS+ NEGATIVE VSS FOR ISSS- 	<b>TEST CIRCUIT 2 Igss1,2</b> POSITIVE VGS FOR IGSS1+ NEGATIVE VGS FOR IGSS1- When FET1 is measured between GATE and SOURCE of FET2 are shorted 
<b>TEST CIRCUIT 3 Vgs(off)</b> When FET1 is measured between GATE and SOURCE of FET2 are shorted 	<b>TEST CIRCUIT 4 Rss(on)</b> Vss/Is 
<b>TEST CIRCUIT 5 VF(ss)1,2</b> When FET1 measured FET2 VGS=4.5V 	<b>TEST CIRCUIT 6 BVdss</b> POSITIVE VSS FOR ISSS+ NEGATIVE VSS FOR ISSS- 
<b>TEST CIRCUIT 7 BVgs01,2</b> POSITIVE VSS FOR ISSS+ NEGATIVE VSS FOR ISSS- When FET1 is measured between GATE and SOURCE of FET2 are shorted 	<b>TEST CIRCUIT 8 Switching time</b> 