ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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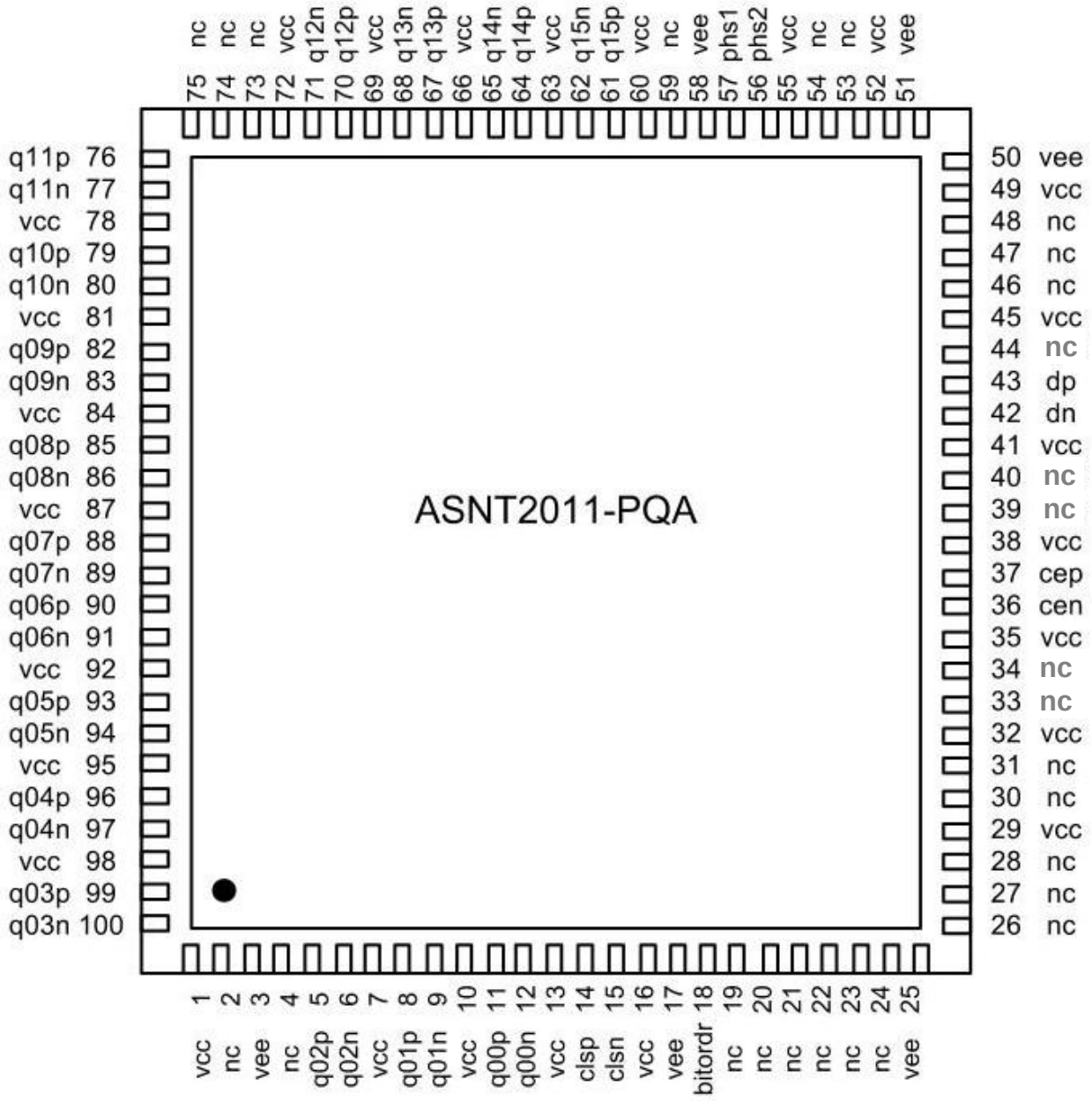
ASNT2011-PQA
DC-17*Gbps* Digital Demultiplexer 1:16 / Deserializer

- Broadband digital deserializer 1-to-16
- Low-power LVDS output data buffers with a proprietary architecture
- Clock-divided-by-16 LVDS output buffer with 90°-step phase selection
- Single +3.3*V* power supply
- Industrial temperature range
- Low power consumption of 730*mW* at the maximum speed
- Standard 100-pin QFN package (12*mm* x 12*mm*)



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DESCRIPTION

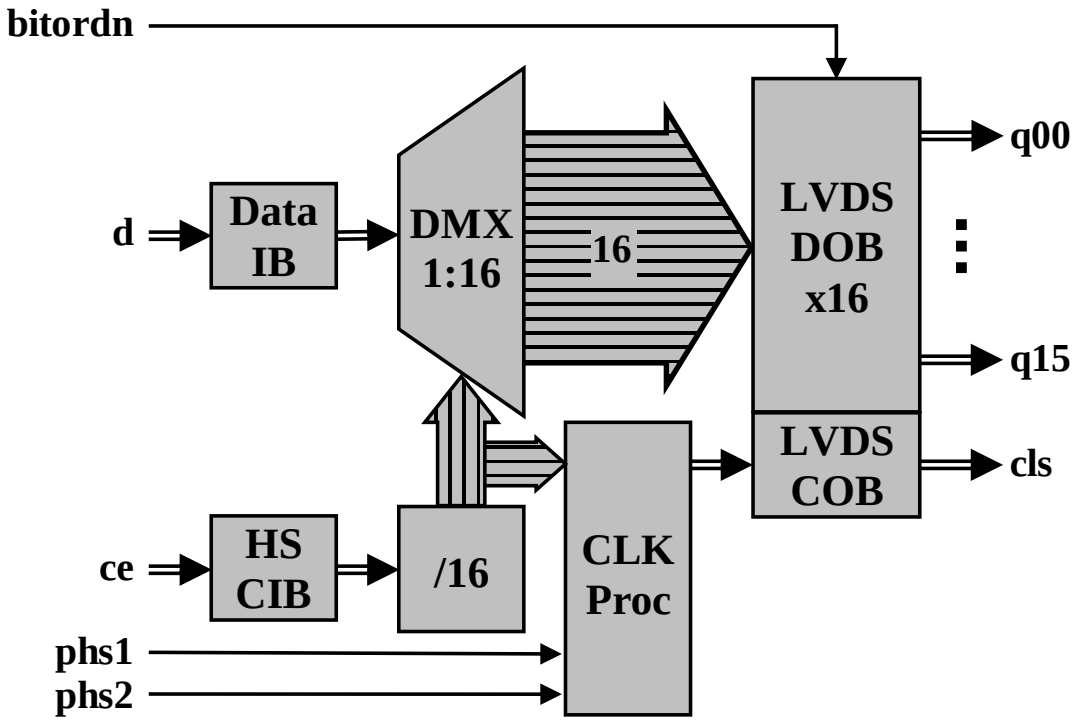

Fig. 1. Functional Block Diagram

ASNT2011-PQA is a low power and high-speed digital 1 to 16 demultiplexer / deserializer IC. The IC shown in Fig. 1 can function seamlessly over input data rates (f_{bit}) ranging from DC to 17*Gbps*.

The main function of ASNT2011-KMA is to demultiplex a serial input data channel d running at a bit rate of f_{bit} into 16 parallel data channels q00-q15 running at a bit rate of $f_{bit}/16$. The high sensitivity data input buffer (Data IB) ensures accurate operation at low input data signal amplitudes. It provides on-chip 50*Ohm* termination to vcc and is designed to be driven by devices with 50*Ohm* source impedance.

During normal operation, the received serial input data is latched into a tree-type demultiplexer DMX1:16 and subsequently deserialized and delivered to the demultiplexer's output as 16-bit wide low-speed parallel words. The output MSB corresponds to q00 when bitordn=0 (default), or to q15 when bitordn=1.

A full rate clock must be provided by an external source ce to the high-speed clock input buffer HS CIB where it is routed to the internal divider-by-16 (/16). The divider provides signaling for DMX1:16 and produces a full rate clock divided-by-16 C16 for the low speed LVDS compliant clock output buffer LVDS COB. The phase of cls can be modified by 90° increments by utilizing pins phs1 and phs2 and the clock processing block CLK Proc.

Sixteen proprietary low-power LVDS output data buffers LVDS DOBx16 are used to deliver the 16 data output signals q00-q15 while a similar LVDS clock output buffer LVDS COB outputs the low-speed clock signal cls.

The deserializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

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Data IB

The Data Input Buffer (Data IB) can process an input CML data signal d with bit rates from DC to f_{bit}. It can also accept a single-ended signal to one of its pins with a threshold voltage applied to the unused pin. Data IB can handle a wide range of input signal amplitudes. The buffer utilizes on-chip single-ended termination of 50*Ohm* to vcc for each input line.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process an external CML clock signal ce with frequencies from DC to f_{bit}. It can also accept a single-ended signal to one of its pins with a threshold voltage applied to the unused pin. HS CIB can handle a wide range of input signal amplitudes. The buffer utilizes on-chip single-ended termination of 50*Ohm* to vcc for each input line.

/16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The high-speed clock delivered by HS CIB is fed into the first divide-by-2 where its output is routed internally to the next divide-by-two circuit and outside of the block to DMX1:16. Other divided down clock signals are formed and routed to DMX1:16 in similar fashion. A full rate clock divided-by-16 C16 is passed on to CLK Proc for additional phase adjustment.

DMX1:16

The 1 to 16 Demultiplexer (DMX1:16) utilizes a tree type architecture that latches in the data stream from Data IB on both edges of a half-rate clock signal supplied by the divider (/16). The high speed data signal is subsequently demultiplexed down and delivered to LVDS DOBx16 in parallel fashion as 16-bit wide words running at a data rate up to $f_{bit}/16$.

CLK Proc

By utilizing the CMOS control pins phs1 and phs2, the phase of cls can be altered as shown in Table 1.

Table 1. Output Clock Phase Selection

phs1	phs2	C16S phase
vee (default)	vee (default)	270°
vee	vcc	180°
vcc	vee	90°
vcc	vcc	0°

LVDS DOBx16

The LVDS Data Output Buffer (LVDS DOBx16) accepts 16-bit wide words from DMX1:16 and converts them into LVDS output signals. Each proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at bit rates up to 2*Gb/s* with a nominal output current of 3.5*mA*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 standards. The output MSB corresponds to q00 when bitordn=0 (default), or to q15 when bitordn=1.

LVDS COB

The LVDS Clock Output Buffer (LVDS COB) receives C16 from CLK Proc and converts it into the LVDS output signal cls. The proprietary low-power LVDS output buffer utilizes a special architecture that ensures

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operation at frequencies up to 2.0*GHz* with a nominal output current of 3.5*mA*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 standards.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		+3.6	*V*
Power Consumption		0.8	*W*
RF Input Voltage Swing (SE)		1.2	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	1, 7, 10, 13, 16, 29, 32, 35, 38, 41, 45, 49, 52, 55, 60, 63, 66, 69, 72, 78, 81, 84, 87, 92, 95, 98
vee	Negative power supply (GND or 0*V*)	3, 17, 25, 50, 51, 58
nc	Not connected pins	2, 4, 19, 20, 21, 22, 23, 24, 26, 27, 28, 30, 31, 33, 34, 39, 40, 44, 46, 47, 48, 53, 54, 59, 73, 74, 75

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dp	43	Input	CML differential data inputs with internal SE 50*Ohm* termination to vcc
dn	42		
cep	37	Input	CML differential clock inputs with internal SE 50*Ohm* termination to vcc
cen	36		
Controls			
phs1	57	LS In., CMOS	Low-speed output clock phase selection (default: both low)
phs2	56		
bitordr	18	LS In., CMOS	Output bit order selection (active: high, q15 is MSB; default: low, q00 is MSB)

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TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
Low-Speed I/Os			
q00n	12	Output	LVDS data outputs
q00p	11		
q01n	9		
q01p	8		
q02n	6		
q02p	5		
q03n	100		
q03p	99		
q04n	97		
q04p	96		
q05n	94		
q05p	93		
q06n	91		
q06p	90		
q07n	89		
q07p	88		
q08n	86		
q08p	85		
q09n	83		
q09p	82		
q10n	80		
q10p	79		
q11n	77		
q11p	76		
q12n	71		
q12p	70		
q13n	68		
q13p	67		
q14n	65		
q14p	64		
q15n	62		
q15p	61		
clsp	14	Output	LVDS clock output, can transmit four different clock phases as defined by phs1 and phs2
clsn	15		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.14	+3.3	+3.47	*V*	±5%
vee		0.0		*V*	External ground
*I*vcc		220		*mA*	
Power consumption		730		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (dp/dn)					
Data Rate	0	17	18	*Gbps*	
Swing p-p (Diff or SE)	0.04		1.2	*V*	Peak-to-peak
CM Voltage Level	vcc -0.8		vcc	*V*	
HS Input Clock (cep/cen)					
Frequency	0.0	17	18	*GHz*	
Swing p-p (Diff or SE)	0.2		1.2	*V*	Peak-to-peak
CM Voltage Level	vcc -0.8		vcc	*V*	
Duty Cycle	40	50	60	*%*	
LS Output Data (q00p/q00n-q15p/q15n)					
Data Rate	0.0	1063	1125	*Mbps*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
LS Output Clock (clsp/clsn)					
Frequency	0.0	1063	1125	*MHz*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
CMOS Control Inputs/Outputs					
Logic “1” level	vcc -0.4			*V*	
Logic “0” level			vee+0.4	*V*	
Timing Parameters					
cls to q0-q15 delay variation		±2.5%			Over the full temperature range

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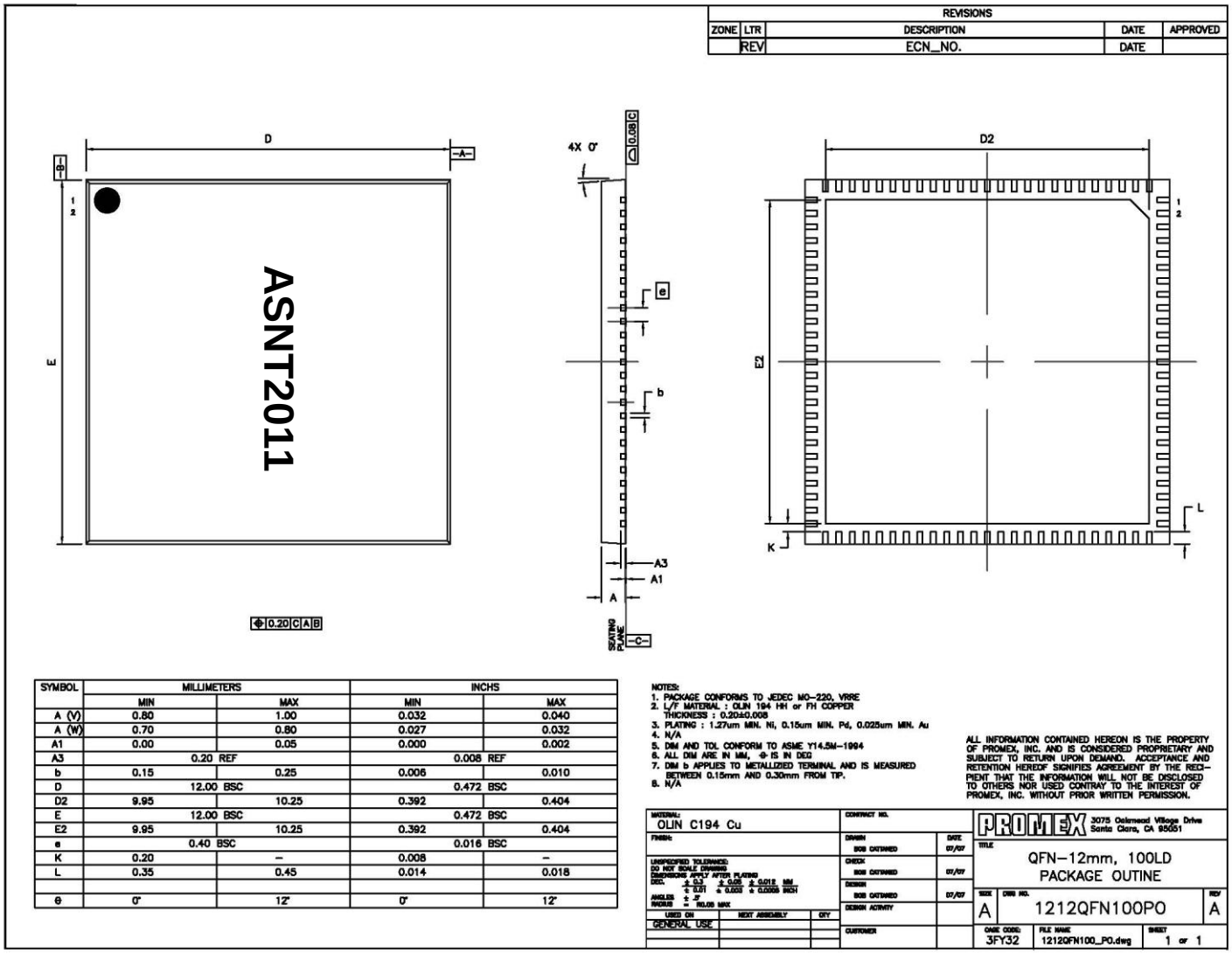
PACKAGE INFORMATION



SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A (V)	0.80	1.00	0.032	0.040
A (W)	0.70	0.80	0.027	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	12.00 BSC		0.472 BSC	
D2	9.95	10.25	0.392	0.404
E	12.00 BSC		0.472 BSC	
E2	9.95	10.25	0.392	0.404
e	0.40 BSC		0.016 BSC	
K	0.20	–	0.008	–
L	0.35	0.45	0.014	0.018
θ	0°	12°	0°	12°

NOTES:
1. PACKAGE CONFORMS TO JEDEC MO-220, VRRE
2. L/F MATERIAL : OLIN 194 HH or FH COPPER THICKNESS : 0.20±0.008
3. PLATING : 1.27um MIN. Ni, 0.15um MIN. Pd, 0.025um MIN. Au
4. N/A
5. DIM AND TOL CONFORM TO ASME Y14.5M-1994
6. ALL DIM ARE IN MM, ⌀ IS IN DEG
7. DIM b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM TIP.
8. N/A

Fig. 2. Package Drawing

Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the vee plain that is ground for the positive supply.

The part's identification label is ASNT2011-PQA. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
2.4.2	05-2020	Updated Package Information
2.3.2	07-2019	Updated Letterhead
2.3.1	10-2013	Corrected pin out drawing Corrected terminal functions (vcc and nc pins)
2.2.1	05-2013	Corrected input voltage characteristics Corrected maximum ratings
2.1.1	09-2012	Corrected input voltage range Corrected format
2.0	04-2012	Added package pin out drawing Added absolute maximum ratings Revised package information section
1.0	01-2009	First release