LM3151/LM3152/LM3153 SIMPLE SWITCHER® CONTROLLER, High Input Voltage Synchronous Step-Down

Check for Samples: LM3151, LM3152, LM3153

FEATURES

- **PowerWise™ Step-down Controller**
- **6V to 42V Wide Input Voltage Range**
- **Fixed Output Voltage of 3.3V**
- **Fixed Switching Frequencies of 250 kHz/500 kHz/750 kHz**
- **No Loop Compensation Required**
- **Fully WEBENCH® Enabled**
- **Low External Component Count**
- **Constant On-Time Control**
- **Ultra-Fast Transient Response**
- **Stable with Low ESR Capacitors**
- **Output Voltage Pre-bias Startup**
- **Valley Current Limit**
- **Programmable Soft-start**

TYPICAL APPLICATIONS

- **Telecom**
- **Networking Equipment**
- **Routers**
- **Security Surveillance**
- **Power Modules**

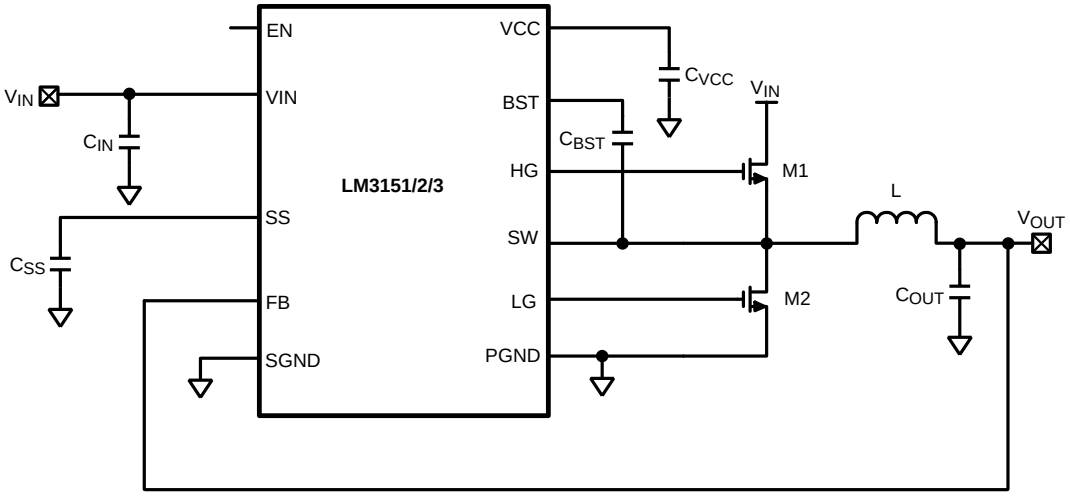
DESCRIPTION

The LM3151/2/3 SIMPLE SWITCHER Controller is an easy to use and simplified step down power controller capable of providing up to 12A of output current in a typical application. Operating with an input voltage range from 6V-42V, the LM3151/2/3 features a fixed output voltage of 3.3V, and features switching frequencies of 250 kHz, 500 kHz, and 750 kHz. The synchronous architecture provides for highly efficient designs. The LM3151/2/3 controller employs a Constant On-Time (COT) architecture with a proprietary Emulated Ripple Mode (ERM) control that allows for the use of low ESR output capacitors, which reduces overall solution size and output voltage ripple. The Constant On-Time (COT) regulation architecture allows for fast transient response and requires no loop compensation, which reduces external component count and reduces design complexity.

Fault protection features such as thermal shutdown, under-voltage lockout, over-voltage protection, short-circuit protection, current limit, and output voltage pre-bias startup allow for a reliable and robust solution.

The LM3151/2/3 SIMPLE SWITCHER concept provides for an easy to use complete design using a minimum number of external components and TI's WEBENCH online design tool. WEBENCH provides design support for every step of the design process and includes features such as external component calculation with a new MOSFET selector, electrical simulation, thermal simulation, and Build-It boards for prototyping.

Typical Application



Connection Diagram

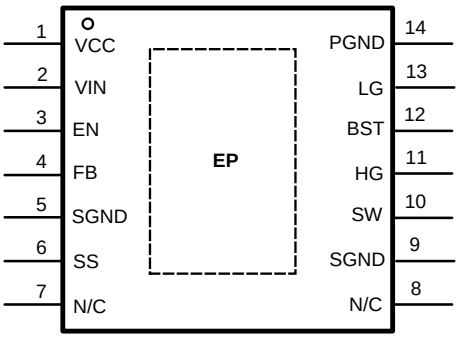


Figure 1. HTSSOP-14

PIN DESCRIPTIONS

Pin	Name	Description	Function
1	VCC	Supply Voltage for FET Drivers	Nominally regulated to 5.95V. Connect a 1 µF to 2.2 µF decoupling capacitor from this pin to ground.
2	VIN	Input Supply Voltage	Supply pin to the device. Nominal input range is 6V to 42V. See ordering information for Vin limitations.
3	EN	Enable	To enable the IC apply a logic high signal to this pin greater than 1.26V typical or leave floating. To disable the part, ground the EN pin.
4	FB	Feedback	Internally connected to the resistor divider network which sets the fixed output voltage. This pin also senses the output voltage faults such a over-voltage and short circuit conditions.
5,9	SGND	Signal Ground	Ground for all internal bias and reference circuitry. Should be connected to PGND at a single point.
6	SS	Soft-Start	An internal 7.7 µA current source charges an external capacitor to provide the soft-start function.
7,8	N/C	Not Connected	Internally not electrically connected. These pins may be left unconnected or connected to ground.
10	SW	Switch Node	Switch pin of controller and high-gate driver lower supply rail. A boost capacitor is also connected between this pin and BST pin
11	HG	High-Side Gate Drive	Gate drive signal to the high-side NMOS switch. The high-side gate driver voltage is supplied by the differential voltage between the BST pin and SW pin.
12	BST	Connection for Bootstrap Capacitor	High-gate driver upper supply rail. Connect a 0.33 µF-0.47 µF capacitor from SW pin to this pin. An internal diode charges the capacitor during the high-side switch off-time. Do not connect to an external supply rail.
13	LG	Low-Side Gate Drive	Gate drive signal to the low-side NMOS switch. The low-side gate driver voltage is supplied by VCC.
14	PGND	Power Ground	Synchronous rectifier MOSFET source connection. Tie to power ground plane. Should be tied to SGND at a single point.
EP	EP	Exposed Pad	Exposed die attach pad should be connected directly to SGND. Also used to help dissipate heat out of the IC.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

VIN to GND	-0.3V to 47V
SW to GND	-3V to 47V
BST to SW	-0.3V to 7V
BST to GND	-0.3V to 52V
All Other Inputs to GND	-0.3V to 7V
ESD Rating (3)	2kV
Storage Temperature Range	-65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test Method is per JESD-22-A114.

OPERATING RATINGS(1)

V_{IN}	6V to 42V
Junction Temperature Range (T_J)	−40°C to + 125°C
EN	0V to 5V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.

ELECTRICAL CHARACTERISTICS

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 18V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Start-Up Regulator, VCC						
V_{CC}		C_{VCC} = 1 µF, 0 mA to 40 mA	**5.65**	5.95	**6.25**	V
V_{IN} - V_{CC}	V_{IN} - V_{CC} Dropout Voltage	I_{VCC} = 2 mA, Vin = 5.5V		40		mV
		I_{VCC} = 30 mA, Vin = 5.5V		330		
I_{VCCL}	V_{CC} Current Limit (1)	V_{CC} = 0V	**65**	100		mA
VCC_{UVLO}	VCC Under-voltage Lockout threshold (UVLO)	VCC Increasing	**4.75**	5.1	**5.40**	V
$V_{CC-UVLO-HYS}$	V_{CC} UVLO Hysteresis	VCC Decreasing		475		mV
$t_{CC-UVLO-D}$	V_{CC} UVLO Filter Delay			3		µs
I_{IN}	Input Operating Current	No Switching		3.6	**5.2**	mA
I_{IN-SD}	Input Operating Current, Device Shutdown	V_{EN} = 0V		32	**55**	µA
GATE Drive						
I_{Q-BST}	Boost Pin Leakage	V_{BST} – V_{SW} = 6V		2		nA
$R_{DS-HG-Pull-Up}$	HG Drive Pull–Up On-Resistance	I_{HG} Source = 200 mA		5		Ω
$R_{DS-HG-Pull-Down}$	HG Drive Pull–Down On-Resistance	I_{HG} Sink = 200 mA		3.4		Ω
$R_{DS-LG-Pull-Up}$	LG Drive Pull–Up On-Resistance	I_{LG} Source = 200 mA		3.4		Ω
$R_{DS-LG-Pull-Down}$	LG Drive Pull–Down On-Resistance	I_{LG} Sink = 200 mA		2		Ω

(1) VCC provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 18V.

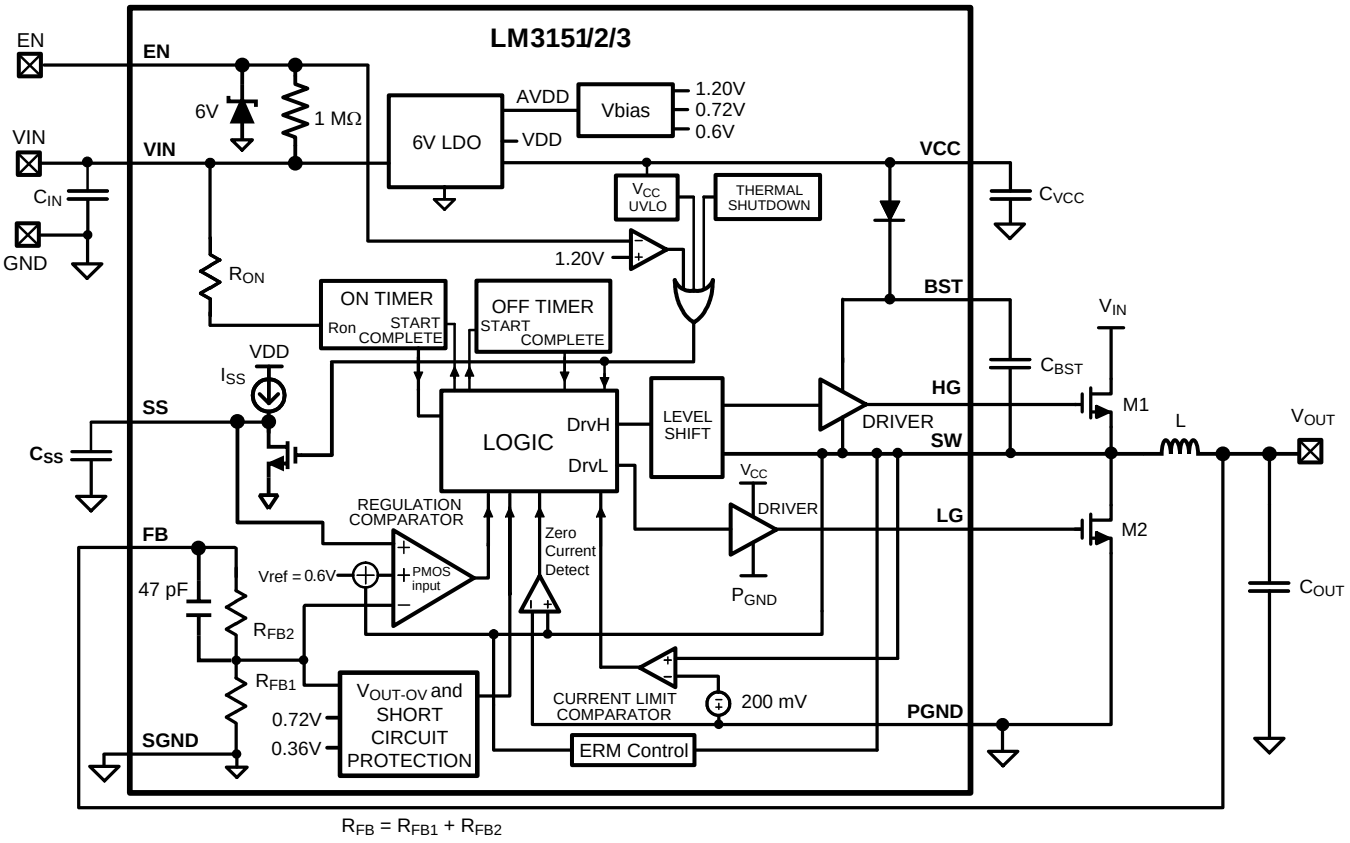
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Soft-Start						
I_{SS}	SS Pin Source Current	V_{SS} = 0V	**5.9**	7.7	**9.5**	mA
I_{SS-DIS}	SS Pin Discharge Current			200		µA
Current Limit						
V_{CL}	Current Limit Voltage Threshold		175	200	225	mV
ON/OFF Timer						
t_{ON-MIN}	ON Timer Minimum Pulse Width			200		ns
t_{OFF}	OFF Timer Minimum Pulse Width			370	**525**	ns
Enable Input						
V_{EN}	EN Pin Input Threshold Trip Point	V_{EN} Rising	**1.14**	1.20	**1.26**	V
V_{EN-HYS}	EN Pin threshold Hysteresis	V_{EN} Falling		120		mV
Boost Diode						
V_f	Forward Voltage	I_{BST} = 2 mA		0.7		V
		I_{BST} = 30 mA		1		V
Thermal Characteristics						
T_{SD}	Thermal Shutdown	Rising		165		°C
	Thermal Shutdown Hysteresis	Falling		15		°C
θ_{JA}	Junction to Ambient	4 Layer JEDEC Printed Circuit Board, 9 Vias, No Air Flow		40		°C/W
		2 Layer JEDEC Printed Circuit Board. No Air Flow		140		
θ_{JC}	Junction to Case	No Air Flow		4		°C/W

ELECTRICAL CHARACTERISTICS 3.3V OUTPUT OPTION

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage		**3.234**	3.3	**3.366**	V
V_{OUT-OV}	Output Voltage Over-Voltage Threshold		**3.83**	4.00	**4.17**	V
V_{IN-MAX}	Maximum Input Voltage (1)	LM3151-3.3		42		V
		LM3152-3.3		33		
		LM3153-3.3		18		
V_{IN-MIN}	Minimum Input Voltage (1)	LM3151-3.3		6		V
		LM3152-3.3		6		
		LM3153-3.3		8		
f_S	Switching Frequency	LM3151-3.3, R_{ON} = 115 kΩ		250		kHz
		LM3152-3.3, R_{ON} = 51 kΩ		500		
		LM3153-3.3, R_{ON} = 32 kΩ		750		
t_{ON}	On-Time	LM3151-3.3, R_{ON} = 115 kΩ		730		ns
		LM3152-3.3, R_{ON} = 51 kΩ		400		
		LM3153-3.3, R_{ON} = 32 kΩ		330		
R_{FB}	FB Resistance to Ground			566		kΩ

(1) The input voltage range is dependent on minimum on-time, off-time, and therefore frequency, and is also affected by optimized MOSFET selection.

SIMPLIFIED BLOCK DIAGRAM



$R_{FB} = R_{FB1} + R_{FB2}$

TYPICAL PERFORMANCE CHARACTERISTICS

Boost Diode Forward Voltage vs. Temperature

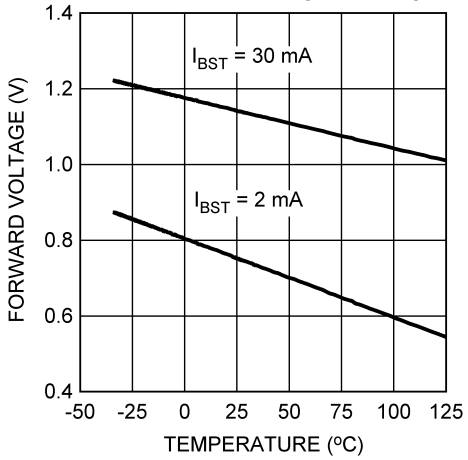


Figure 2.

Quiescent Current vs. Temperature

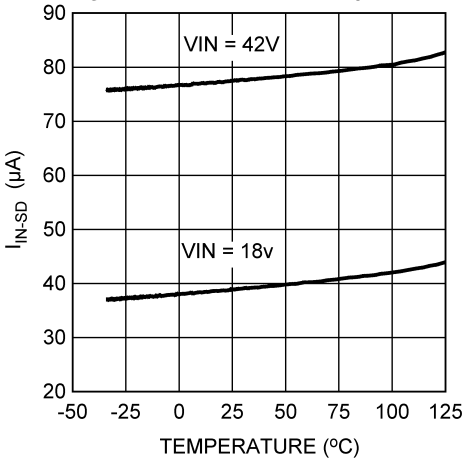


Figure 3.

Soft-Start Current vs. Temperature

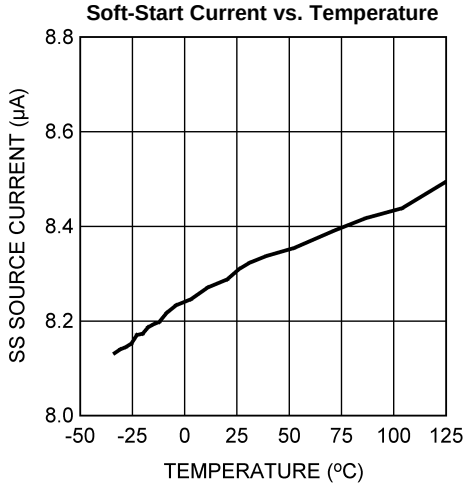


Figure 4.

VCC Current Limit vs. Temperature

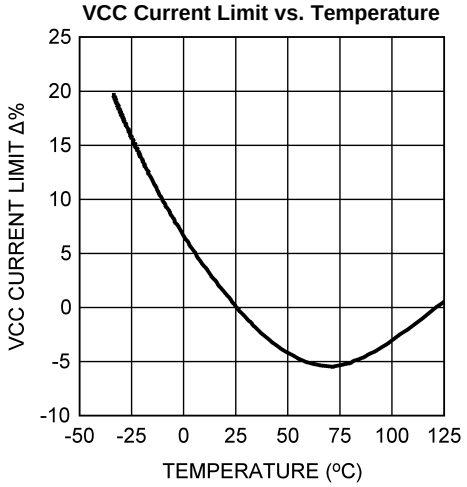


Figure 5.

VCC Dropout vs. Temperature

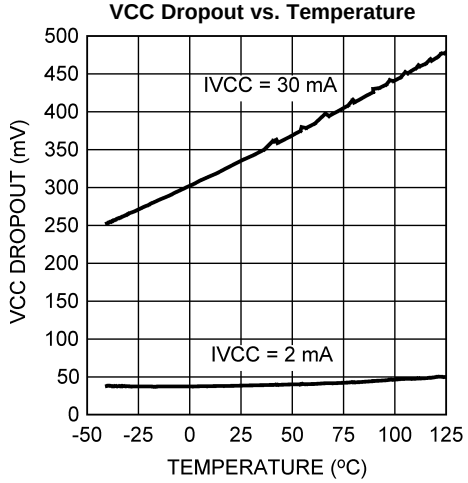


Figure 6.

VCC vs. Temperature

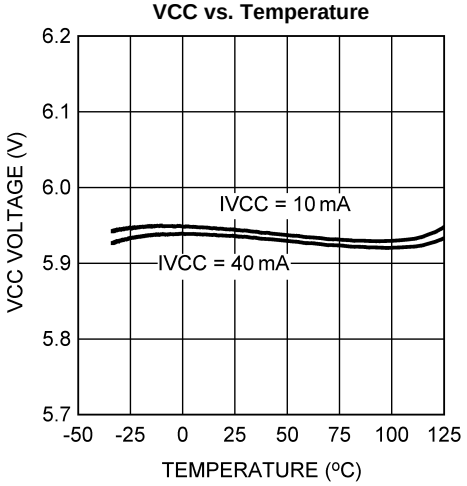


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VCL vs. Temperature

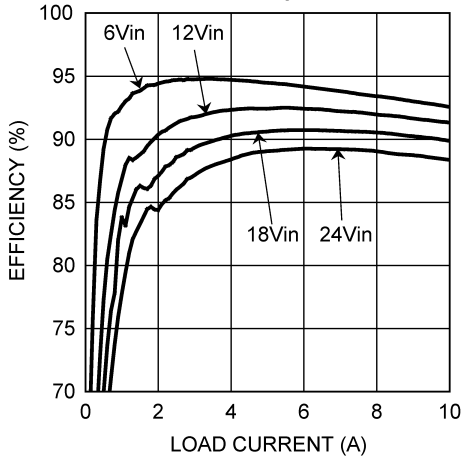


Figure 8.

On-Time vs. Temperature (250 kHz)

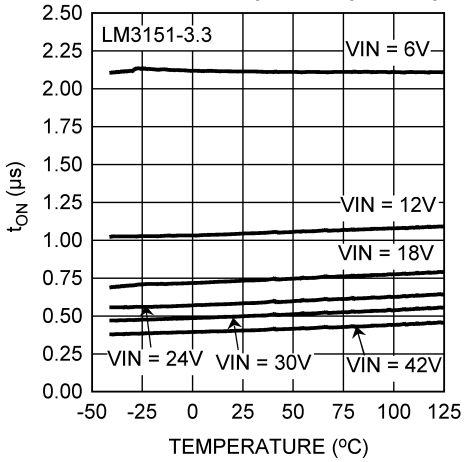


Figure 9.

On-Time vs. Temperature (500 kHz)

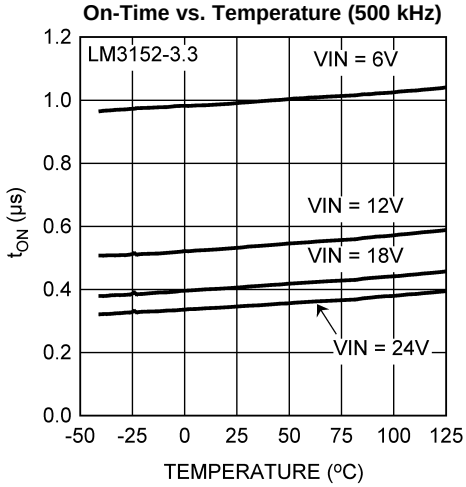


Figure 10.

On-Time vs. Temperature (750 kHz)

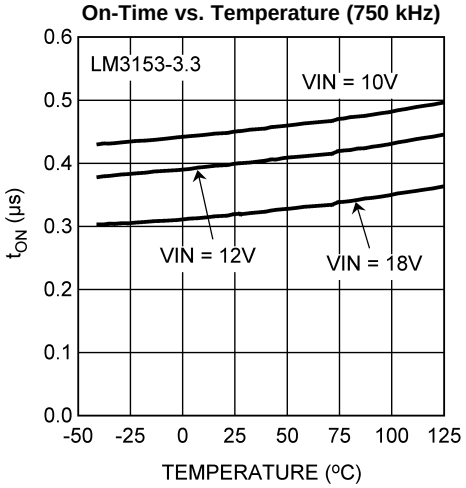


Figure 11.

THEORY OF OPERATION

The LM3151/2/3 synchronous step-down SIMPLE SWITCHER Controller employs a Constant On-Time (COT) architecture which is a derivative of the hysteretic control scheme. COT relies on a fixed switch on-time to regulate the output. The on-time of the high-side switch is set internally by resistor R_{ON}. The LM3151/2/3 automatically adjusts the on-time inversely with the input voltage to maintain a constant frequency. Assuming an ideal system and V_{IN} is much greater than 1V, the following approximations can be made:

The on-time, t_{ON}:

$$t_{ON} = \frac{K \times R_{ON}}{V_{IN}}$$

where

- K = 100 pC
- R_{ON} is specified in the electrical characteristics table

Control is based on a comparator and the on-timer, with the output voltage feedback (FB) attenuated and then compared with an internal reference of 0.6V. If the attenuated FB level is below the reference, the high-side switch is turned on for a fixed time, t_{ON}, which is determined by the input voltage and the internal resistor, R_{ON}. Following this on-time, the switch remains off for a minimum off-time, t_{OFF}, as specified in the Electrical Characteristics table or until the attenuated FB voltage is less than 0.6V. This switching cycle will continue while maintaining regulation. During continuous conduction mode (CCM), the switching frequency depends only on duty cycle and on-time. The duty cycle can be calculated as:

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_S \approx \frac{V_{OUT}}{V_{IN}}$$

Where the switching frequency of a COT regulator is:

$$f_S = \frac{V_{OUT}}{K \times R_{ON}}$$

Typical COT hysteretic controllers need a significant amount of output capacitor ESR to maintain a minimum amount of ripple at the FB pin in order to switch properly and maintain efficient regulation. The LM3151/2/3 however utilizes proprietary, Emulated Ripple Mode Control Scheme (ERM) that allows the use of ceramic output capacitors without additional equivalent series resistance (ESR) compensation. Not only does this reduce the need for output capacitor ESR, but also significantly reduces the amount of output voltage ripple seen in a typical hysteretic control scheme. The output ripple voltage can become so low that it is comparable to voltage-mode and current-mode control schemes.

Regulation Comparator

The output voltage is sampled through the FB pin and then divided down by two internal resistors and compared to the internal reference voltage of 0.6V by the error comparator. In normal operation, an on-time period is initiated when the sampled output voltage at the input of the error comparator falls below 0.6V. The high-side switch stays on for the specified on-time, causing the sampled voltage on the error comparator input to rise above 0.6V. After the on-time period, the high-side switch stays off for the greater of the following:

1. Minimum off time as specified in the electrical characteristics table
2. The error comparator sampled voltage falls below 0.6V

Over-Voltage Comparator

The over-voltage comparator is provided to protect the output from over-voltage conditions due to sudden input line voltage changes or output loading changes. The over-voltage comparator continuously monitors the attenuated FB voltage versus a 0.72V internal reference. If the voltage at FB rises above 0.72V the on-time pulse is immediately terminated. This condition can occur if the input or the output load changes suddenly. Once the over-voltage protection is activated, the HG and LG signals remain off until the attenuated FB voltage falls below 0.72V.

Current Limit

Current limit detection occurs during the off-time by monitoring the current through the low-side switch. If during the off-time the current in the low-side switch exceeds the user defined current limit value, the next on-time cycle is immediately terminated. Current sensing is achieved by comparing the voltage across the low-side switch against an internal reference value, V_{CL}, of 200 mV. If the voltage across the low-side switch exceeds 200 mV, the current limit comparator will trigger logic to terminate the next on-time cycle. The current limit I_{CL}, can be determined as follows:

$$V_{CL}(T_j) = V_{CL} \times [1 + 3.3 \times 10^{-3} \times (T_j - 27)]$$

$$I_{CL}(T_j) = \frac{V_{CL}(T_j)}{R_{DS(ON)max}}$$

where

- I_{OCL} is the user-defined average output current limit value
- $R_{DS(ON)max}$ is the resistance value of the low-side FET at the expected maximum FET junction temperature
- V_{CL} is the internal current limit reference voltage
- T_j is the junction temperature of the LM3151/2/3

Figure 12 illustrates the inductor current waveform. During normal operation, the output current ripple is dictated by the switching of the FETs. The current through the low-side switch, I_{valley}, is sampled at the end of each switching cycle and compared to the current limit threshold voltage, V_{CL}. The valley current can be calculated as follows:

$$I_{valley} = I_{OUT} - \frac{\Delta I_L}{2}$$

where

- I_{OUT} is the average output current
- ΔI_L is the peak-to-peak inductor ripple current

If an overload condition occurs, the current through the low-side switch will increase which will cause the current limit comparator to trigger the logic to skip the next on-time cycle. The IC will then try to recover by checking the valley current during each off-time. If the valley current is greater than or equal to I_{CL}, then the IC will keep the low-side FET on and allow the inductor current to further decay.

Throughout the whole process, regardless of the load current, the on-time of the controller will stay constant and thereby the positive ripple current slope will remain constant. During each on-time the current ramps up an amount equal to:

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L}$$

The valley current limit feature prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay following any overload conditions.

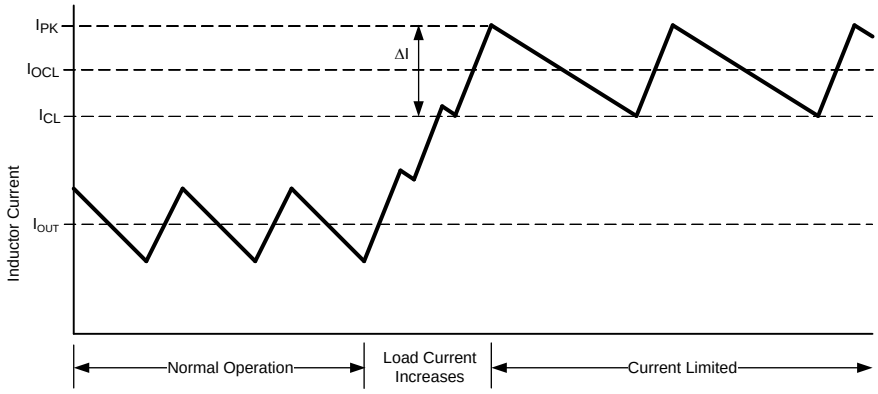


Figure 12. Inductor Current - Current Limit Operation

Short-Circuit Protection

The LM3151/2/3 will sense a short-circuit on the output by monitoring the output voltage. When the attenuated feedback voltage has fallen below 60% of the reference voltage, V_{ref} x 0.6 (≈ 0.36V), short-circuit mode of operation will start. During short-circuit operation, the SS pin is discharged and the output voltage will fall to 0V. The SS pin voltage, V_{SS}, is then ramped back up at the rate determined by the SS capacitor and I_{SS} until V_{SS} reaches 0.7V. During this re-ramp phase, if the short-circuit fault is still present the output current will be equal to the set current limit. Once the soft-start voltage reaches 0.7V the output voltage is sensed again and if the attenuated V_{FB} is still below V_{ref} x 0.6 then the SS pin is discharged again and the cycle repeats until the short-circuit fault is removed.

Soft-Start

The soft-start (SS) feature allows the regulator to gradually reach a steady-state operating point, which reduces start-up stresses and current surges. At turn-on, while VCC is below the under-voltage threshold, the SS pin is internally grounded and V_{OUT} is held at 0V. The SS capacitor is used to slowly ramp V_{FB} from 0V to it's final output voltage as programmed by the internal resistor divider. By changing the soft-start capacitor value, the duration of start-up can be changed accordingly. The start-up time can be calculated using the following equation:

$$t_{SS} = \frac{V_{ref} \times C_{SS}}{I_{SS}}$$

where

- t_{SS} is measured in seconds
- V_{ref} = 0.6V
- I_{SS} is the soft-start pin source current, which is typically 7.7 µA (refer to electrical characteristics table)

An internal switch grounds the SS pin if VCC is below the under-voltage lockout threshold, if a thermal shutdown occurs, or if the EN pin is grounded. By using an externally controlled switch, the output voltage can be shut off by grounding the SS pin.

During startup the LM3151/2/3 will operate in diode emulation mode, where the low-side gate LG will turn off and remain off when the inductor current falls to zero. Diode emulation mode allows for start up into a pre-biased output voltage. When soft-start is greater than 0.7V, the LM3151/2/3 will remain in continuous conduction mode. During diode emulation mode at current limit the low-gate will remain off when the inductor current is off.

The soft start time should be greater than the rise time specified by,

$$t_{SS} \geq (V_{OUT} \times C_{OUT}) / (I_{OCL} - I_{OUT})$$

Enable/Shutdown

The EN pin can be activated by either leaving the pin floating due to an internal pull up resistor to VIN or by applying a logic high signal to the EN pin of 1.26V or greater. The LM3151/2/3 can be remotely shut down by taking the EN pin below 1.02V. Low quiescent shutdown is achieved when V_{EN} is less than 0.4V. During low quiescent shutdown the internal bias circuitry is turned off.

The LM3151/2/3 has certain fault conditions that can trigger shutdown, such as over-voltage protection, current limit, under-voltage lockout, or thermal shutdown. During shutdown, the soft-start capacitor is discharged. Once the fault condition is removed, the soft-start capacitor begins charging, allowing the part to start up in a controlled fashion. In conditions where there may be an open drain connection to the EN pin, it may be necessary to add a 1000 pF bypass capacitor to this pin. This will help decouple noise from the EN pin and prevent false disabling.

Thermal Protection

The LM3151/2/3 should be operated such that the junction temperature does not exceed the maximum operating junction temperature. An internal thermal shutdown circuit, which activates at 165°C (typical), takes the controller to a low-power reset state by disabling the buck switch and the on-timer, and grounding the SS pin. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature falls back below 150°C the SS pin is released and normal operation resumes.

Design Guide

The design guide provides the equations required to design with the LM3151/2/3 SIMPLE SWITCHER Controller. WEBENCH design tool can be used with or in place of this section for a more complete and simplified design process.

1. Define Power Supply Operating Conditions

a. Maximum and Minimum DC Input voltage
b. Maximum Expected Load Current during normal operation
c. Target Switching Frequency

2. Determine which IC Controller to Use

The desired input voltage range will determine which version of the LM3151/2/3 controller will be chosen. The higher switching frequency options allow for physically smaller inductors but efficiency may decrease.

3. Determine Inductor Required Using Figure 13

To use the nomograph below calculate the inductor volt-microsecond constant ET from the following formula:

$$ET = (Vinmax - V_{OUT}) \times \frac{V_{OUT}}{Vinmax} \times \frac{1000}{f_S} \ (V \times \mu s)$$

where

- f_S is in kHz units

The intersection of the Load Current and the Volt-microseconds lines on the chart below will determine which inductors are capable for use in the design. The chart shows a sample of parts that can be used. The offline calculator tools and WEBENCH will fully calculate the requirements for the components needed for the design.

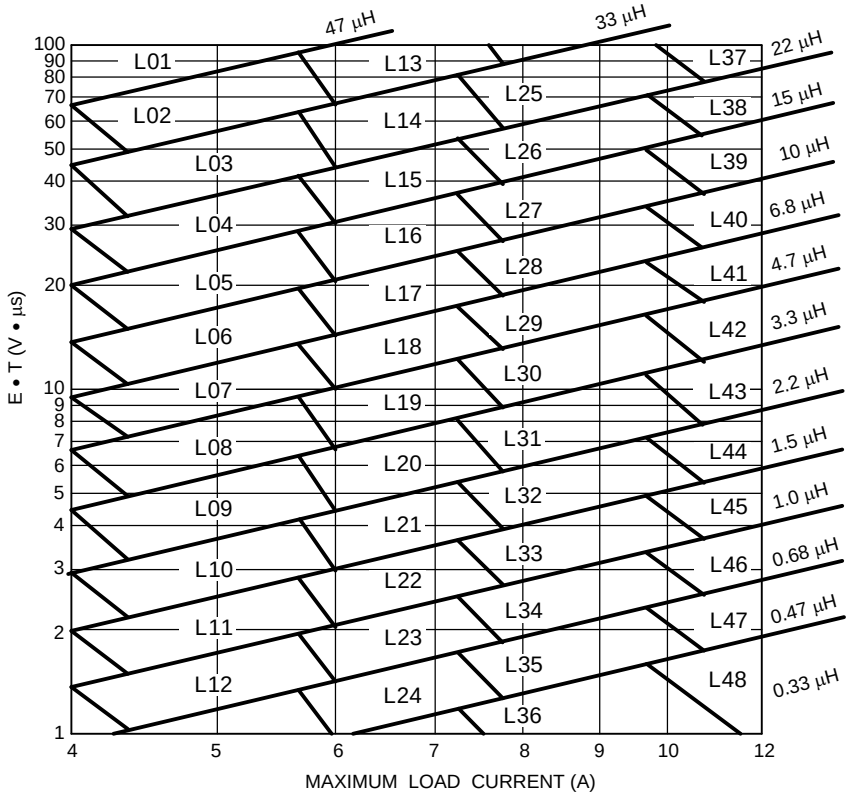


Figure 13. Inductor Nomograph

Table 1. Inductor Selection Table

Inductor Designator	Inductance (µH)	Current (A)	Part Name	Vendor
L01	47	7-9		
L02	33	7-9	SER2817H-333KL	COILCRAFT
L03	22	7-9	SER2814H-223KL	COILCRAFT
L04	15	7-9	7447709150	WURTH
L05	10	7-9	RLF12560T-100M7R5	TDK
L06	6.8	7-9	B82477-G4682-M	EPCOS
L07	4.7	7-9	B82477-G4472-M	EPCOS
L08	3.3	7-9	DR1050-3R3-R	COOPER
L09	2.2	7-9	MSS1048-222	COILCRAFT
L10	1.5	7-9	SRU1048-1R5Y	BOURNS
L11	1	7-9	DO3316P-102	COILCRAFT
L12	0.68	7-9	DO3316H-681	COILCRAFT
L13	33	9-12		
L14	22	9-12	SER2918H-223	COILCRAFT
L15	15	9-12	SER2814H-153KL	COILCRAFT
L16	10	9-12	7447709100	WURTH
L17	6.8	9-12	SPT50H-652	COILCRAFT
L18	4.7	9-12	SER1360-472	COILCRAFT
L19	3.3	9-12	MSS1260-332	COILCRAFT
L20	2.2	9-12	DR1050-2R2-R	COOPER
L21	1.5	9-12	DR1050-1R5-R	COOPER
L22	1	9-12	DO3316H-102	COILCRAFT
L23	0.68	9-12		
L24	0.47	9-12		
L25	22	12-15	SER2817H-223KL	COILCRAFT
L26	15	12-15		
L27	10	12-15	SER2814L-103KL	COILCRAFT
L28	6.8	12-15	7447709006	WURTH
L29	4.7	12-15	7447709004	WURTH
L30	3.3	12-15		
L31	2.2	12-15		
L32	1.5	12-15	MLC1245-152	COILCRAFT
L33	1	12-15		
L34	0.68	12-15	DO3316H-681	COILCRAFT
L35	0.47	12-15		
L36	0.33	12-15	DR73-R33-R	COOPER
L37	22	15-		
L38	15	15-	SER2817H-153KL	COILCRAFT
L39	10	15-	SER2814H-103KL	COILCRAFT
L40	6.8	15-		
L41	4.7	15-	SER2013-472ML	COILCRAFT
L42	3.3	15-	SER2013-362L	COILCRAFT
L43	2.2	15-		
L44	1.5	15-	HA3778-AL	COILCRAFT
L45	1	15-	B82477-G4102-M	EPCOS
L46	0.68	15-		
L47	0.47	15-		

Table 1. Inductor Selection Table (continued)

Inductor Designator	Inductance (µH)	Current (A)	Part Name	Vendor
L48	0.33	15-		

4. Determine Output Capacitance

Typical hysteretic COT converters similar to the LM3151/2/3 require a certain amount of ripple that is generated across the ESR of the output capacitor and fed back to the error comparator. Emulated Ripple Mode control built into the LM3151/2/3 will recreate a similar ripple signal and thus the requirement for output capacitor ESR will decrease compared to a typical Hysteretic COT converter. The emulated ripple is generated by sensing the voltage signal across the low-side FET and is then compared to the FB voltage at the error comparator input to determine when to initiate the next on-time period.

$$C_{Omin} = 70 / (f_s^2 \times L) \quad (1)$$

The maximum ESR allowed to prevent over-voltage protection during normal operation is:

$$ESR_{max} = (80\ mV \times L) / ET_{min}$$

ET_{min} is calculated using V_{IN-MIN}

The minimum ESR must meet both of the following criteria:

$$ESR_{min} \geq (15\ mV \times L) / ET_{max}$$

$$ESR_{min} \geq [ET_{max} / (V_{IN} - V_{OUT})] / C_O$$

ET_{max} is calculated using V_{IN-MAX}.

Any additional parallel capacitors should be chosen so that their effective impedance will not negatively attenuate the output ripple voltage.

5. MOSFET Selection

The high-side and low-side FETs must have a drain to source (V_{DS}) rating of at least 1.2 x V_{IN}.

The gate drive current from VCC must not exceed the minimum current limit of VCC. The drive current from VCC can be calculated with:

$$I_{VCCdrive} = Q_{gtotal} \times f_S$$

where

- Q_{gtotal} is the combined total gate charge of the high-side and low-side FETs

Use the following equations to calculate the current limit, I_{CL}, as shown in Figure 12.

$$V_{CL}(T_j) = V_{CL} \times [1 + 3.3 \times 10^{-3} \times (T_j - 27)]$$

$$I_{CL}(T_j) = \frac{V_{CL}(T_j)}{R_{DS(ON)max}}$$

where

- T_j is the junction temperature of the LM3151/2/3

The plateau voltage of the FET V_{GS} vs Q_g curve, as shown in Figure 14 must be less than VCC - 750 mV.

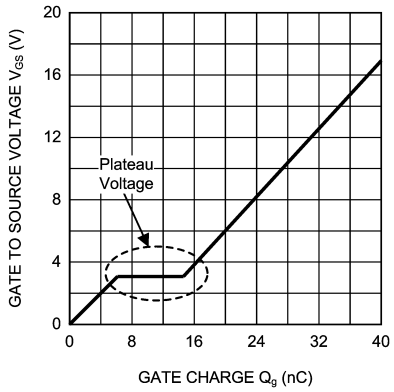


Figure 14. Typical MOSFET Gate Charge Curve

See following design example for estimated power dissipation calculation.

6. Calculate Input Capacitance

The main parameters for the input capacitor are the voltage rating, which must be greater than or equal to the maximum DC input voltage of the power supply, and its rms current rating. The maximum rms current is approximately 50% of the maximum load current.

$$C_{IN} = \frac{Iomax \times D \times (1-D)}{f_S \times \Delta V_{IN-MAX}}$$

where

- ΔV_{IN-MAX} is the maximum allowable input ripple voltage

A good starting point for the input ripple voltage is 5% of V_{IN}.

When using low ESR ceramic capacitors on the input of the LM3151/2/3 a resonant circuit can be formed with the impedance of the input power supply and parasitic impedance of long leads/PCB traces to the LM3151/2/3 input capacitors. It is recommended to use a damping capacitor under these circumstances, such as aluminum electrolytic that will prevent ringing on the input. The damping capacitor should be chosen to be approximately 5 times greater than the parallel ceramic capacitors combination. The total input capacitance should be greater than 10 times the input inductance of the power supply leads/pcb trace. The damping capacitor should also be chosen to handle its share of the rms input current which is shared proportionately with the parallel impedance of the ceramic capacitors and aluminum electrolytic at the LM3151/2/3 switching frequency.

The C_{BYP} capacitor should be placed directly at the VIN pin. The recommended value is 0.1 µF.

7. Calculate Soft-Start Capacitor

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{ref}}$$

where

- t_{SS} is the soft-start time in seconds
- V_{ref} = 0.6V

8. C_{VCC}, and C_{BST} and C_{EN}

C_{VCC} should be placed directly at the VCC pin with a recommended value of 1 µF to 2.2 µF. For input voltage ranges that include voltages below 8V a 1 µF capacitor must be used for C_{VCC}. C_{BST} creates a voltage used to drive the gate of the high-side FET. It is charged during the SW off-time. The recommended value for C_{BST} is 0.47 µF. The EN bypass capacitor, C_{EN}, recommended value is 1000 pF when driving the EN pin from open drain type of signal.

Design Example

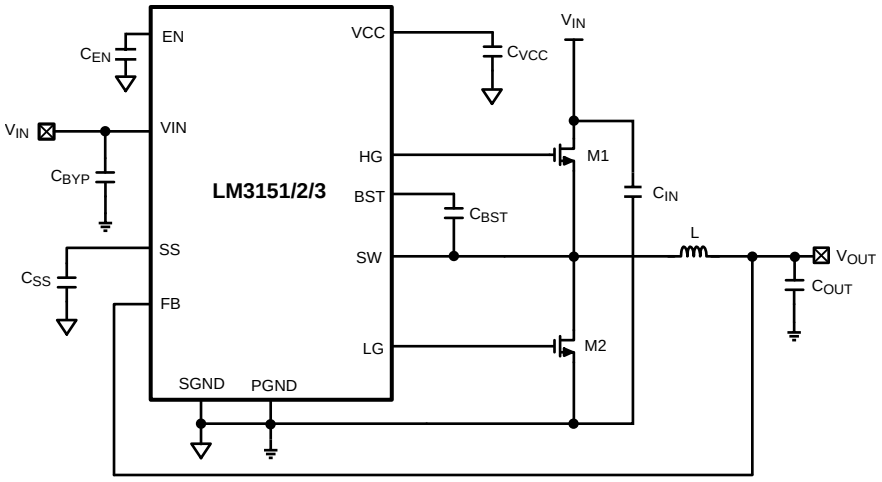


Figure 15. Design Example Schematic

1.Define Power Supply Operating Conditions

a. V_{OUT} = 3.3V
b. V_{IN-MIN} = 6V, V_{IN-TYP} = 12V, V_{IN-MAX} = 24V
c. Typical Load Current = 12A, Max Load Current = 15A
d. Soft-Start time t_{SS} = 5 ms

2. Determine which IC Controller to Use

The LM3151 and LM3152 allow for the full input voltage range. However, from buck converter basic theory, the higher switching frequency will allow for a smaller inductor. Therefore, the LM3152-3.3 500 kHz part is chosen so that a smaller inductor can be used.

3. Determine Inductor Required

a. ET = (24-3.3) x (3.3/24) x (1000/500) = 5.7 V µs
b. From the inductor nomograph a 12A load and 5.7 V µs calculation corresponds to a L44 type of inductor.
c. Using the inductor designator L44 in Table 1 the Coilcraft HA3778-AL 1.65 µH inductor is chosen.

4. Determine Output Capacitance

The voltage rating on the output capacitor should be greater than or equal to the output voltage. As a rule of thumb most capacitor manufacturers suggests not to exceed 90% of the capacitor rated voltage. In the case of multilayer ceramics the capacitance will tend to decrease dramatically as the applied voltage is increased towards the capacitor rated voltage. The capacitance can decrease by as much as 50% when the applied voltage is only 30% of the rated voltage. The chosen capacitor should also be able to handle the rms current which is equal to:

$$Irmsco = I_{OUT} \times \frac{r}{\sqrt{12}} \quad (2)$$

For this design the chosen ripple current ratio, r = 0.3, represents the ratio of inductor peak-to-peak current to load current Iout. A good starting point for ripple ratio is 0.3 but it is acceptable to choose r between 0.25 to 0.5. The nomographs in this datasheet all use 0.3 as the ripple current ratio.

$$Irmsco = 12 \times \frac{0.3}{\sqrt{12}} \quad (3)$$

I_{rmsco} = 1A

t_{ON} = (3.3V/12V) / 500 kHz = 550 ns

Minimum output capacitance is:

C_{Omin} = 70 / (f_S^2 x L)

C_{Omin} = 70 / (500 kHz^2 x 1.65 µH) = 169 µF

The maximum ESR allowed to prevent over-voltage protection during normal operation is:

ESR_{max} = (80 mV x L) / ET

ESR_{max} = (80 mV x 1.65 µH) / 5.7 V µs

ESR_{max} = 23 mΩ

The minimum ESR must meet both of the following criteria:

ESR_{min} ≥ (15 mV x L) / ET

ESR_{min} ≥ [ET / (V_{IN} - V_{OUT})] / C_O

ESR_{min} ≥ (15 mV x 1.65 µH) / 5.7 V µs = 4.3 mΩ

ESR_{min} ≥ [5.7 V µs / (12 - 3.3)] / 169 µF = 3.9 mΩ

Based on the above criteria two 150 µF polymer aluminum capacitors with a ESR = 12 mΩ each for a effective ESR in parallel of 6 mΩ was chosen from Panasonic. The part number is EEF-UE0J151P.

5. MOSFET Selection

The LM3151/2/3 are designed to drive N-channel MOSFETs. For a maximum input voltage of 24V we should choose N-channel MOSFETs with a maximum drain-source voltage, V_{DS}, greater than 1.2 x 24V = 28.8V. FETs with maximum V_{DS} of 30V will be the first option. The combined total gate charge Q_{gtotal} of the high-side and low-side FET should satisfy the following:

$Q_{gtotal} \leq I_{VCCL} / f_s$ (4)

$Q_{gtotal} \leq 65\ mA / 500\ kHz$ (5)

$Q_{gtotal} \leq 130\ n$

where

- I_{VCCL} is the minimum current limit of VCC over the temperature range, specified in the electrical characteristics table

The MOSFET gate charge Q_g is gathered from reading the V_{GS} vs Q_g curve of the MOSFET datasheet at the V_{GS} = 5V for the high-side, M1, MOSFET and V_{GS} = 6V for the low-side, M2, MOSFET.

The Renesas MOSFET RJK0305DPB has a gate charge of 10 nC at V_{GS} = 5V, and 12 nC at V_{GS} = 6V. This combined gate charge for a high-side, M1, and low-side, M2, MOSFET 12 nC + 10 nC = 22 nC is less than 130 nC calculated Q_{gtotal}.

The calculated MOSFET power dissipation must be less than the max allowed power dissipation, Pdmax, as specified in the MOSFET datasheet. An approximate calculation of the FET power dissipated Pd, of the high-side and low-side FET is given by:

High-Side MOSFET

$Pcond = I_{out}^2 \times R_{DS(ON)} \times D$

$$Psw = \frac{1}{2} \times V_{in} \times I_{out} \times Q_{gd} \times f_s \times \left(\frac{8.5}{Vcc - Vth} + \frac{6.8}{Vth} \right)$$

$Pdh = Pcond + Psw$

$Pcond = 12^2 \times 0.01 \times 0.275 = 0.396W$

$$Psw = \frac{1}{2} \times 12 \times 12 \times 1.5\ nC \times 500\ kHz \times \left(\frac{8.5}{6 - 2.5} + \frac{6.8}{2.5} \right) = 0.278W$$

$Pdh = 0.396 + 0.278 = 0.674W$

The max power dissipation of the RJK0305DPB is rated as 45W for a junction temperature that is 125°C higher than the case temperature and a thermal resistance from the FET junction to case, θ_{JC}, of 2.78°C/W.

When the FET is mounted onto the PCB, the PCB will have some additional thermal resistance such that the total system thermal resistance of the FET package and the PCB, θ_{JA}, is typically in the range of 30°C/W for this type of FET package. The max power dissipation, Pdmax, with the FET mounted onto a PCB with a 125°C junction temperature rise above ambient temperature and θ_{JA} = 30°C/W, can be estimated by:

Pdmax = 125°C / 30°C/W = 4.1W

The system calculated Pdh of 0.674W is much less than the FET Pdmax of 4.1W and therefore the RJK0305DPB max allowable power dissipation criteria is met.

Low-Side MOSFET

Primary loss is conduction loss given by:

$P_{dl} = I_{out}^2 \times R_{DS(ON)} \times (1-D) = 122 \times 0.01 \times (1-0.275) = 1W$

Pdl is also less than the Pdmax specified on the RJK0305DPB MOSFET datasheet.

However, it is not always necessary to use the same MOSFET for both the high-side and low-side. For most applications it is necessary to choose the high-side MOSFET with the lowest gate charge and the low-side MOSFET is chosen for the lowest allowed $R_{DS(ON)}$. The plateau voltage of the FET V_{GS} vs Q_g curve must be less than VCC - 750 mV.

The current limit, I_{OCL}, is calculated by estimating the $R_{DS(ON)}$ of the low-side FET at the maximum junction temperature of 100°C. Then the following calculation of I_{OCL} is:

$I_{OCL} = I_{CL} + \Delta I_L / 2$

I_{CL} = 200 mV / 0.014 = 14.2A

I_{OCL} = 14.2A + 3.6 / 2 = 16A

6. Calculate Input Capacitance

The input capacitor should be chosen so that the voltage rating is greater than the maximum input voltage which for this example is 24V. Similar to the output capacitor, the voltage rating needed will depend on the type of capacitor chosen. The input capacitor should also be able to handle the input rms current which is approximately 0.5 x I_{OUT}. For this example the rms input current is approximately 0.5 x 12A = 6A.

The minimum capacitance with a maximum 5% input ripple ΔV_{IN-MAX} = (0.05 x 12) = 0.6V:

C_{IN} = [12 x 0.275 x (1-0.275)] / [500 kHz x 0.6] = 8 µF

To handle the large input rms current 2 ceramic capacitors are chosen at 10 µF each with a voltage rating of 50V and case size of 1210, that can handle 3A of rms current each. A 100 µF aluminum electrolytic is chosen to help dampen input ringing.

C_{BYP} = 0.1 µF ceramic with a voltage rating greater than maximum V_{IN}

7. Calculate Soft-Start Capacitor

The soft start-time should be greater than the input voltage rise time and also satisfy the following equality to maintain a smooth transition of the output voltage to the programmed regulation voltage during startup.

$t_{SS} \geq (V_{OUT} \times C_{OUT}) / (I_{OCL} - I_{OUT})$

5 ms > (3.3V x 300 µF) / (1.2 x 12A - 12A)

5 ms > 0.412 ms

The desired soft-start time, t_{SS}, of 5 ms satisfies the equality as shown above. Therefore, the soft-start capacitor, C_{SS}, is calculated as:

C_{SS} = (7.7 µA x 5 ms) / 0.6V = 0.064 µF

Let C_{SS} = 0.068 µF, which is the next closest standard value. This should be a ceramic cap with a voltage rating greater than 10V.

8. C_{VCC}, C_{EN}, and C_{BST}

C_{VCC} = 1µF ceramic with a voltage rating greater than 10V

C_{EN} = 1000 pF ceramic with a voltage rating greater than 10V

C_{BST} = 0.47 µF ceramic with a voltage rating greater than 10V

Bill of Materials

Designator	Value	Parameters	Manufacturer	Part Number
C_{BST}	0.47 µF	Ceramic, X7R, 16V, 10%	TDK	C2012X7R1C474K
C_{BYP}	0.1 µF	Ceramic, X7R, 50V, 10%	TDK	C2012X7R1H104K
C_{EN}	1000 pF	Ceramic, X7R, 50V, 10%	TDK	C1608X7R1H102K
C_{IN1}	100 µF	AL, EEV-FK, 63V, 20%	Panasonic	EEV-FK1J101P
C_{IN2}, C_{IN3}	10 µF	Ceramic, X5R, 35V, 10%	Taiyo Yuden	GMK325BJ106KN-T
C_{OUT1}, C_{OUT2}	150 µF	AL, UE, 6.3V, 20%	Panasonic	EEF-UE0J151R
C_{SS}	0.068 µF	Ceramic, 16V, 10%		0603YC683KAT2A
C_{VCC}	1 µF	Ceramic, X7R, 16V, 10%	Kemet	C0805C105K4RACTU
L1	1.65 µH	Shielded Drum Core, A, 2.53 mΩ	Coilcraft Inc.	HA3778-AL
M1, M2	30V	8 nC, $R_{DS(ON)}$ @4.5V = 10 mΩ	Renesas	RJK0305DB
U1			Texas Instruments	LM3152MH-3.3

PCB Layout Considerations

It is good practice to layout the power components first, such as the input and output capacitors, FETs, and inductor. The first priority is to make the loop between the input capacitors and the source of the low side FET to be very small and tie the grounds of each directly to each other and then to the ground plane through vias. As shown in the figure below, when the input cap ground is tied directly to the source of the low side FET, parasitic inductance in the power path, along with noise coupled into the ground plane, are reduced.

The switch node is the next item of importance. The switch node should be made only as large as required to handle the load current. There are fast voltage transitions occurring in the switch node at a high frequency, and if the switch node is made too large it may act as an antennae and couple switching noise into other parts of the circuit. For high power designs it is recommended to use a multi-layer board. The FET's are going to be the largest heat generating devices in the design, and as such, care should be taken to remove the heat. On multi layer boards using exposed-pad packages for the FET's such as the power-pak SO-8, vias should be used under the FETs to the same plane on the interior layers to help dissipate the heat and cool the FETs. For the typical single FET Power-Pak type FETs the high-side FET DAP is Vin. The Vin plane should be copied to the other interior layers to the bottom layer for maximum heat dissipation. Likewise, the DAP of the low-side FET is connected to the SW node and it's shape should be duplicated to the interior layers down to the bottom layer for maximum heat dissipation.

See the Evaluation Board application note AN-1900 (literature number (SNVA371) for an example of a typical multilayer board layout, and the Demonstration Board Reference Design App Note for a typical 2 layer board layout. Each design allows for single sided component mounting.

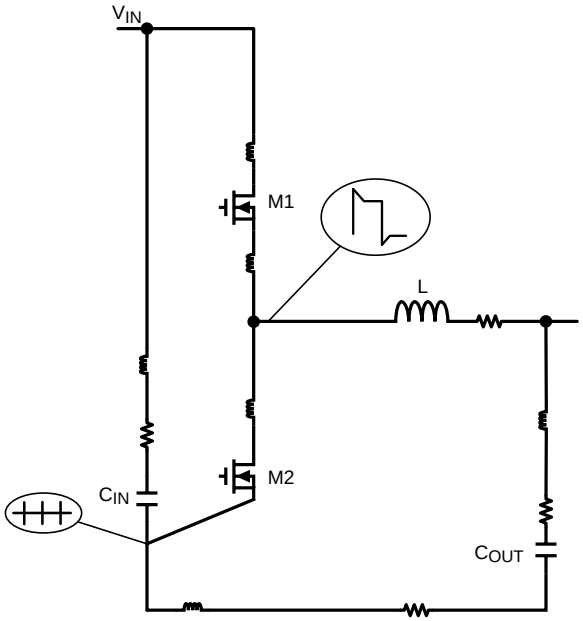


Figure 16. Schematic of Parasitics

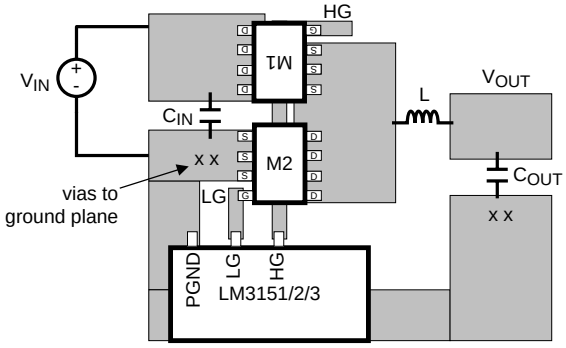


Figure 17. PCB Placement of Power Stage

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3151MH-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3151 -3.3	Samples
LM3151MHE-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3151 -3.3	Samples
LM3151MHX-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3151 -3.3	Samples
LM3152MH-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3152 -3.3	Samples
LM3152MHE-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3152 -3.3	Samples
LM3152MHX-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3152 -3.3	Samples
LM3153MH-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3153 -3.3	Samples
LM3153MHE-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3153 -3.3	Samples
LM3153MHX-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3153 -3.3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

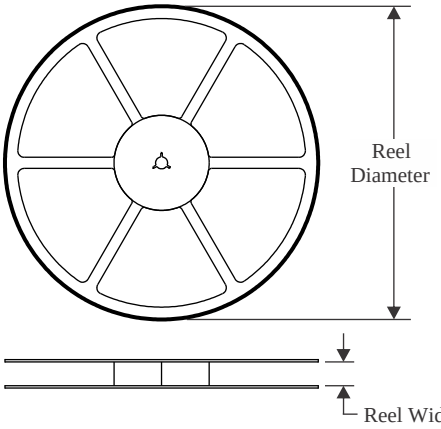
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

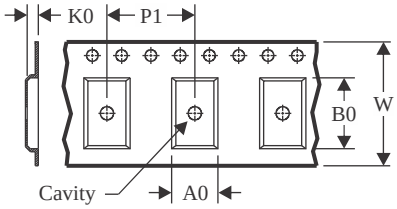
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

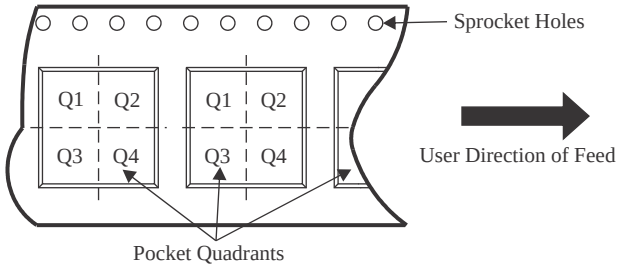


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

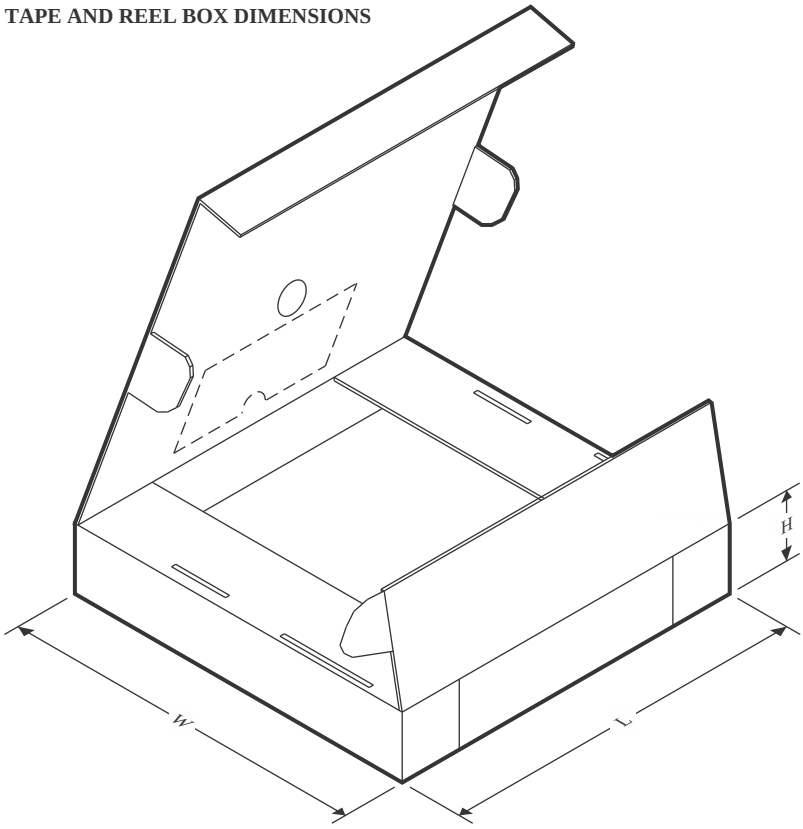
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3151MHE-3.3/NOPB	HTSSOP	PWP	14	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM3151MHX-3.3/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM3152MHE-3.3/NOPB	HTSSOP	PWP	14	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM3152MHX-3.3/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM3153MHE-3.3/NOPB	HTSSOP	PWP	14	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM3153MHX-3.3/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

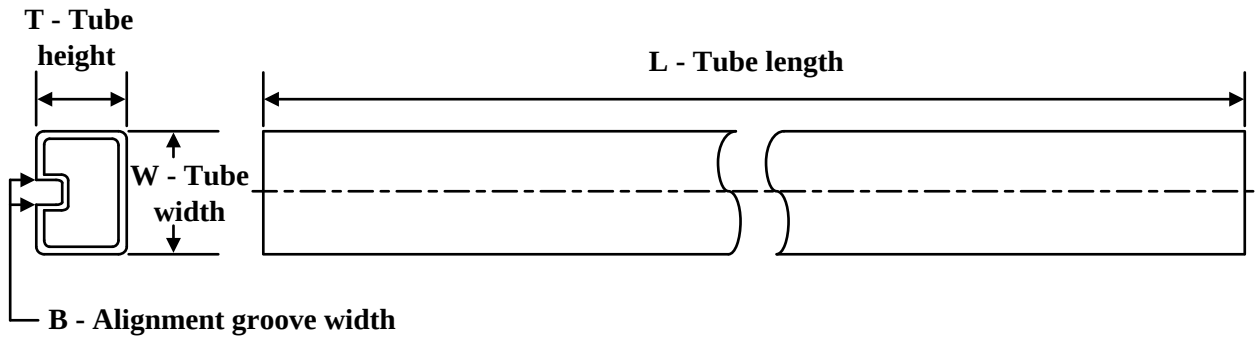
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

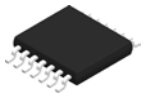
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3151MHE-3.3/NOPB	HTSSOP	PWP	14	250	208.0	191.0	35.0
LM3151MHX-3.3/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM3152MHE-3.3/NOPB	HTSSOP	PWP	14	250	208.0	191.0	35.0
LM3152MHX-3.3/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM3153MHE-3.3/NOPB	HTSSOP	PWP	14	250	208.0	191.0	35.0
LM3153MHX-3.3/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM3151MH-3.3/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM3152MH-3.3/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM3153MH-3.3/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06

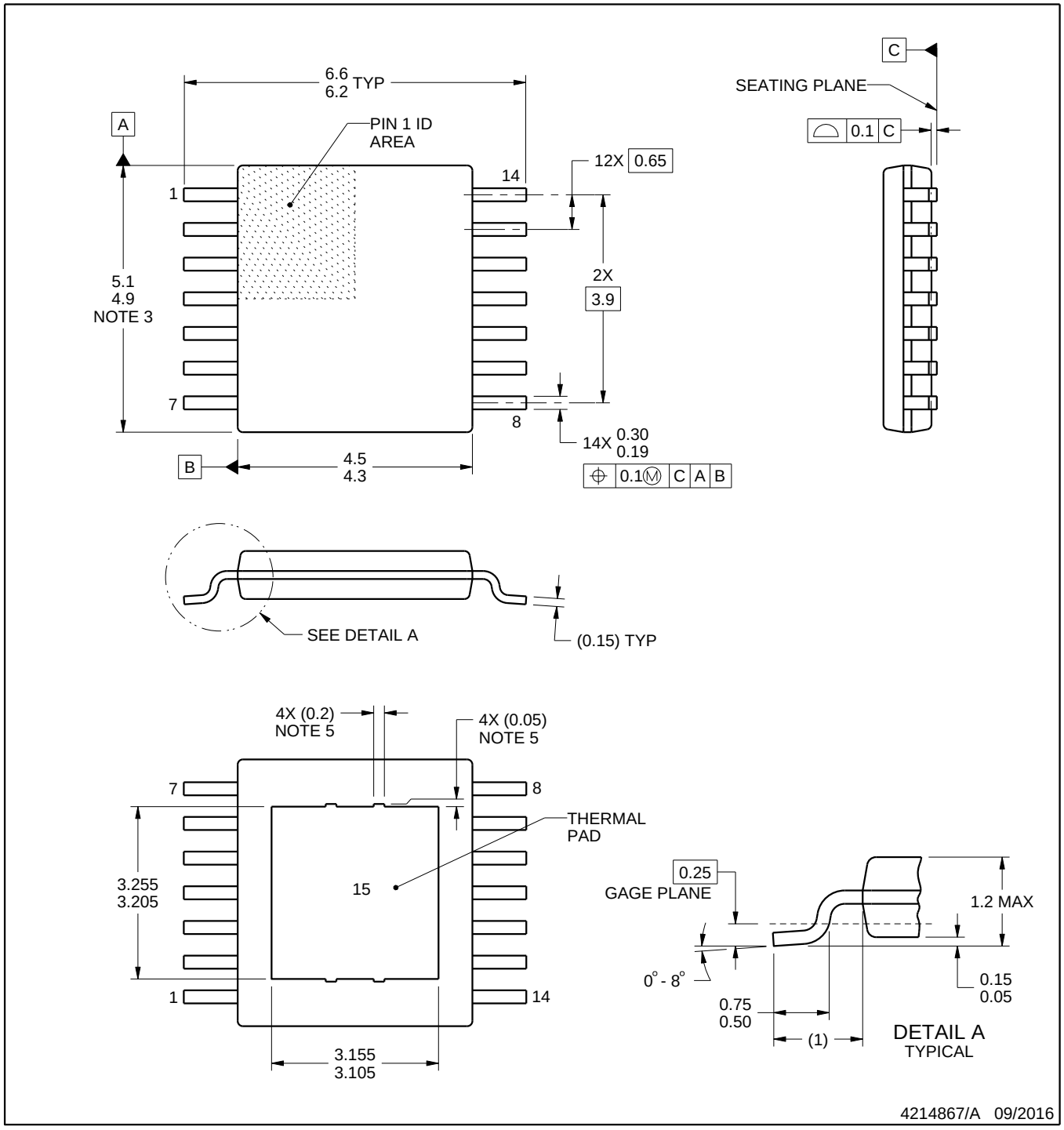


PACKAGE OUTLINE

PWP0014A

PowerPAD™ TSSOP - 1.2 mm max height

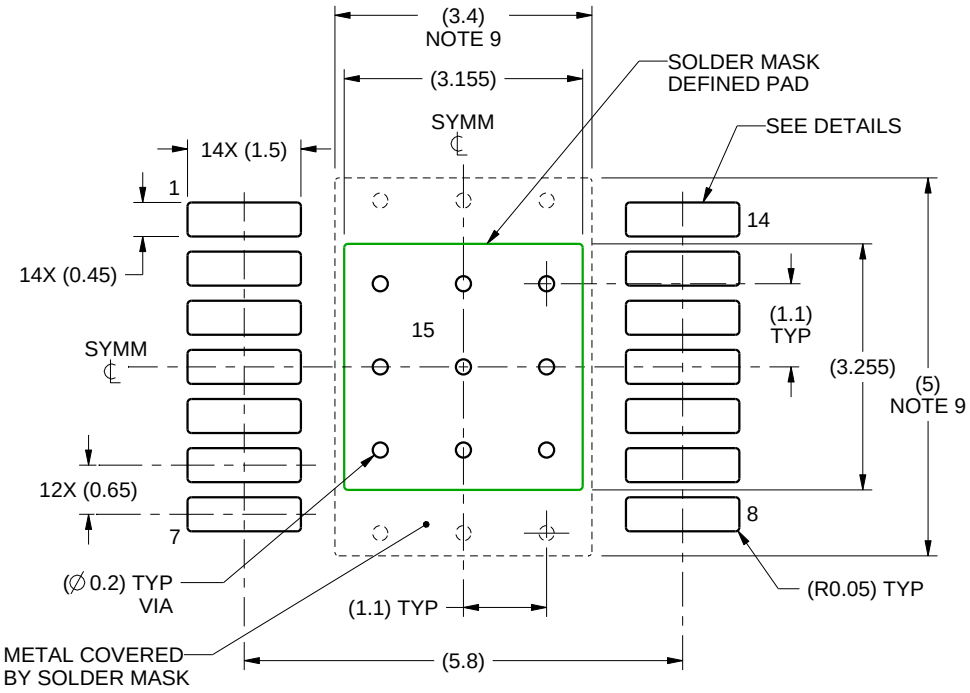
PLASTIC SMALL OUTLINE



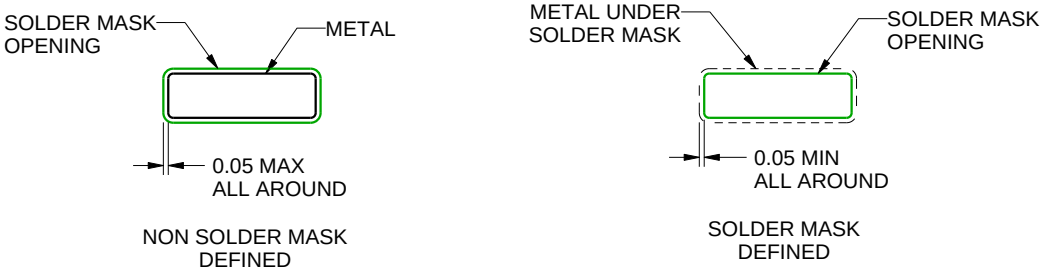
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-14

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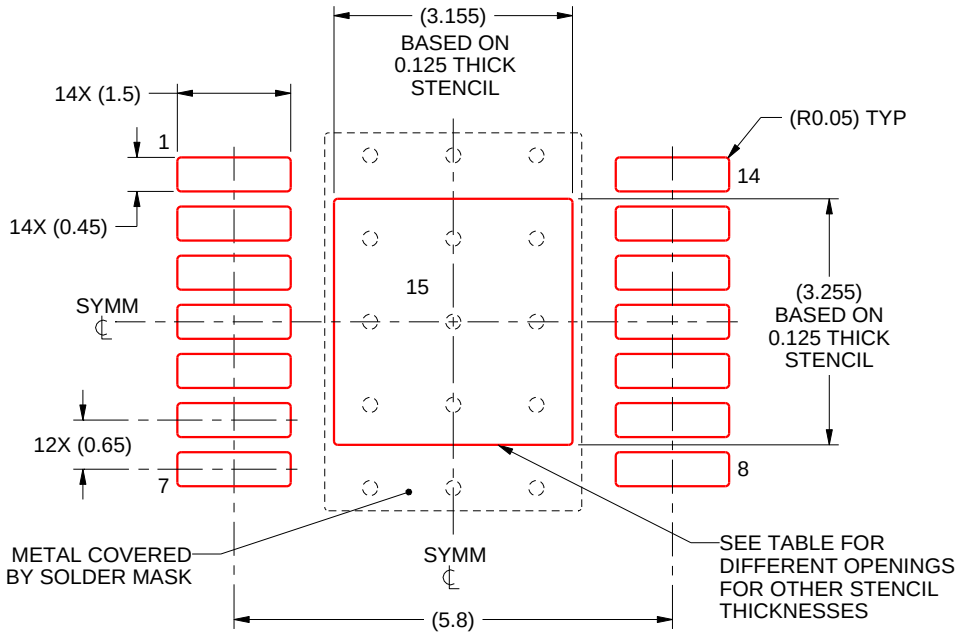
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.53 X 3.64
0.125	3.155 X 3.255 (SHOWN)
0.15	2.88 X 2.97
0.175	2.67 X 2.75

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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