

# SN54259, SN54LS259B, SN74259, SN74LS259B 8-BIT ADDRESSABLE LATCHES

SDLS086 – DECEMBER 1983 – REVISED MARCH 1988

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplified Expansion
- Expandable for N-Bit Applications
- Four District Functional Modes
- Package Options Include Ceramic Chip Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

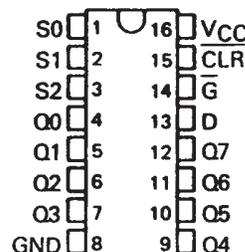
## description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

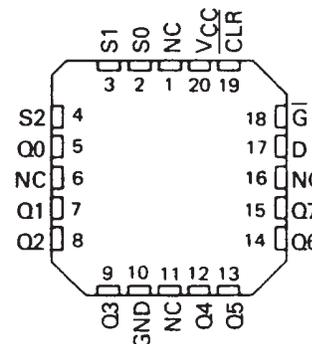
Four distinct modes of operation are selectable by controlling the clear (CLR) and enable (G) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, enable  $\bar{G}$  should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54259 and SN54LS259B are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74259 and SN74LS259B are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54259, SN54LS259B . . . J OR W PACKAGE  
SN74259 . . . N PACKAGE  
SN74LS259B . . . D OR N PACKAGE  
(TOP VIEW)

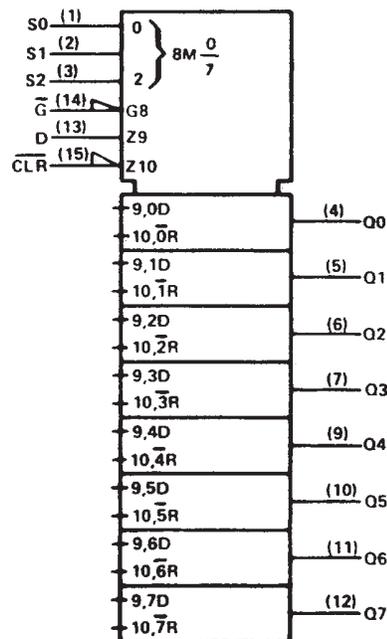


SN54LS259B . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1988, Texas Instruments Incorporated



recommended operating conditions

	SN54259			SN74259			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-800			-800	$\mu A$
Low-level output current, $I_{OL}$			16			16	mA
Width of clear or enable pulse, $t_w$	15			15			ns
Setup time, $t_{su}$	Data	15 $\uparrow$		15 $\uparrow$			ns
	Address	5 $\uparrow$		5 $\uparrow$			
Hold time, $t_h$	Data	0 $\uparrow$		0 $\uparrow$			ns
	Address	20 $\uparrow$		20 $\uparrow$			
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}C$

$\uparrow$ The arrow indicates that the rising edge of the enable pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS $\dagger$	SN54259		SN74259		UNIT
			MIN	TYP $\ddagger$	MAX	MIN	
$V_{IH}$	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage					0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = 12 \text{ mA}$			-1.5	-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu A$	2.4	3.4		2.4 3.4	V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2 0.4		0.2 0.4	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	1	mA
$I_{IH}$	High-level input current	$\bar{G}$			80	80	$\mu A$
		Other inputs	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		40	40	
$I_{IL}$	Low-level input current	$\bar{G}$			-3.2	-3.2	mA
		Other inputs	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6	-1.6	
$I_{OS}$	Short-circuit output current $\S$	$V_{CC} = \text{MAX}$	-18	-57	-18	-57	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX},$ See Note 2		60 90		60 90	mA

$\dagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

$\ddagger$  All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$ .

$\S$  Not more than one output should be shorted at a time.

NOTE 2:  $I_{CC}$  is measured with the inputs grounded and the outputs open.

switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$t_{PHL}$	$\bar{CLR}$	Any Q	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Note 3		16	25	ns		
$t_{PLH}$	Data	Any Q			14	24			
$t_{PHL}$				Address	Any Q		11	20	ns
$t_{PLH}$		15				28			
$t_{PHL}$	$\bar{G}$	Any Q					17	28	ns
$t_{PLH}$							12	20	
$t_{PHL}$					11	20	ns		

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

# SN54LS259B, SN74LS259B 8-BIT ADDRESSABLE LATCHES

SDLS086 – DECEMBER 1983 – REVISED MARCH 1988

## recommended operating conditions

		SN54LS259B			SN74LS259B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-0.4			-0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$t_w$	Pulse duration	$\overline{G}$ low		17			17	ns
		$\overline{CLR}$ low		10			10	
$t_{su}$	Set up time	Data before $\overline{G} \uparrow$		20			20	ns
		Address before $\overline{G} \uparrow$		17			17	
		Address before $\overline{G} \downarrow$		0			0	
$t_h$	Hold time	Data after $\overline{G} \uparrow$		0			0	ns
		Address after $\overline{G} \uparrow$		0			0	
$T_A$	Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS259B			SN74LS259B			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX}$ , $I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 8 \text{ mA}$			0.35	0.5		
$I_I$	$V_{CC} = \text{MAX}$ , $V_I = 7 \text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$			20			20	μA
$I_{IL}$	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS} \S$	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
$I_{CC}$	$V_{CC} = \text{MAX}$ , See Note 2		27	36		22	36	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and duration short-circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with the inputs grounded and the outputs open.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

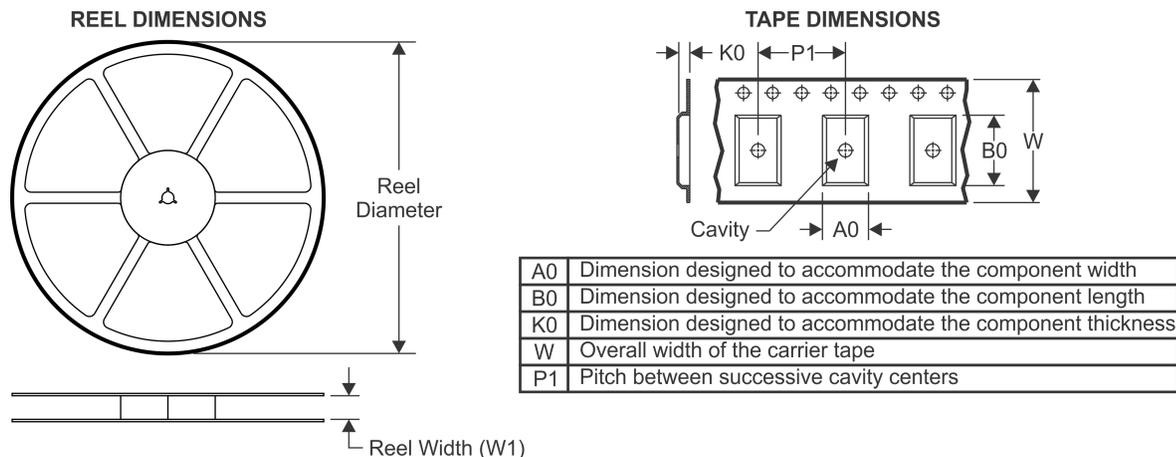
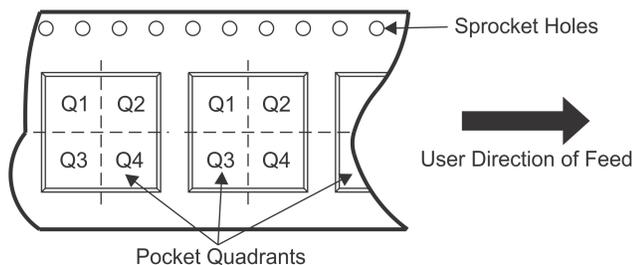
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}$	$\overline{CLR}$	Any Q	$C_L = 15 \text{ pF}$ , See Note 3 $R_L = 2 \text{ k}\Omega$ ,		12	18	ns
$t_{PLH}$	Data	Any Q			19	30	
$t_{PHL}$	Address	Any Q			13	20	ns
$t_{PLH}$					17	27	
$t_{PHL}$	$\overline{G}$	Any Q			14	20	ns
$t_{PLH}$					15	24	
$t_{PHL}$					15	24	

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

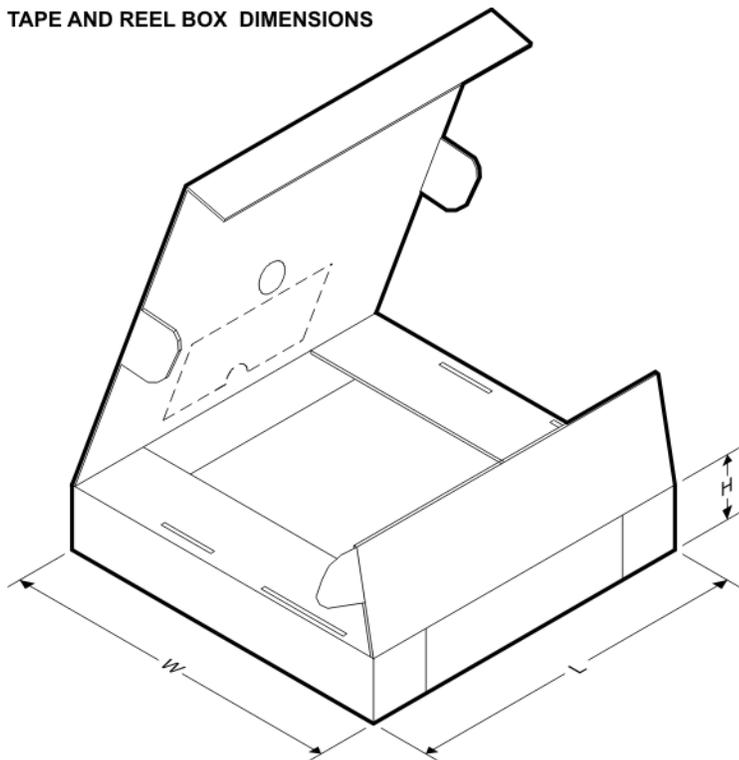
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


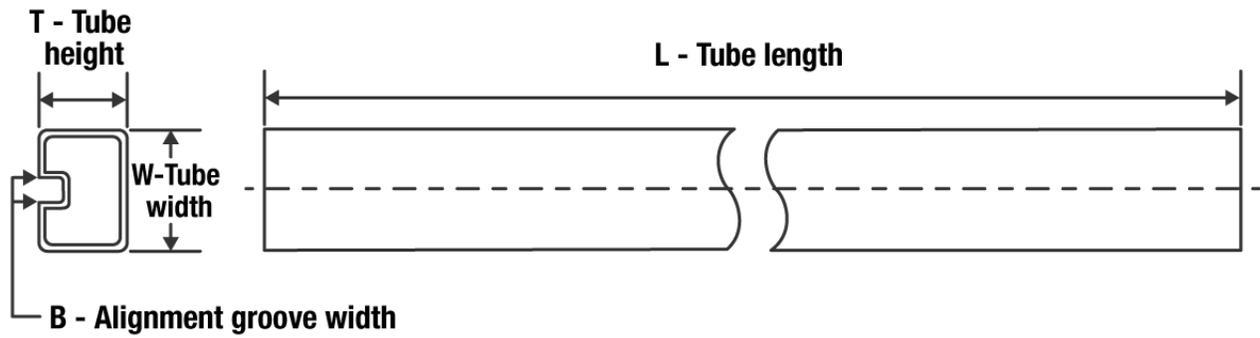
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS259BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS259BDR	SOIC	D	16	2500	340.5	336.1	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LS259BD	D	SOIC	16	40	507	8	3940	4.32
SN74LS259BN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS259BN	N	PDIP	16	25	506	13.97	11230	4.32

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated