# IGBT - Field Stop II / 4 Lead

This Insulated Gate Bipolar Transistor (IGBT) features a robust and cost effective Field Stop II Trench construction, and provides superior performance in demanding switching applications, offering both low on state voltage and minimal switching loss. In addition, this new device is packaged in a TO–247–4L package that provides significant reduction in E<sub>on</sub> Losses compared to standard TO–247–3L package. The IGBT is well suited for UPS and solar applications. Incorporated into the device is a soft and fast co–packaged free wheeling diode with a low forward voltage.

#### **Features**

- Extremely Efficient Trench with Field Stop Technology
- $T_{Jmax} = 175^{\circ}C$
- Improved Gate Control Lowers Switching Losses
- Separate Emitter Drive Pin
- TO-247-4L for Minimal E<sub>on</sub> Losses
- Optimized for High Speed Switching
- This is a Pb–Free Devices

#### **Typical Applications**

- Solar Inverters
- Uninterruptible Power Supplies (UPS)
- Neutral Point Clamp Topology

### **ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-emitter voltage	V <sub>CES</sub>	1200	V
Collector current @ Tc = 25°C @ Tc = 100°C	IC	100 25	Α
Pulsed collector current, T <sub>pulse</sub> limited by T <sub>Jmax</sub>	I <sub>CM</sub>	100	Α
Diode forward current @ Tc = 25°C @ Tc = 100°C	lF	100 25	Α
Diode pulsed current, T <sub>pulse</sub> limited by T <sub>Jmax</sub>	I <sub>FM</sub>	100	Α
Gate-emitter voltage Transient gate-emitter voltage (T <sub>pulse</sub> = 5 µs, D < 0.10)	V <sub>GE</sub>	±20 ±30	V
Power Dissipation @ Tc = 25°C @ Tc = 100°C	P <sub>D</sub>	385 192	W
Operating junction temperature range	$T_J$	-55 to +175	°C
Storage temperature range	T <sub>stg</sub>	-55 to +175	°C
Lead temperature for soldering, 1/8" from case for 5 seconds	T <sub>SLD</sub>	260	°C

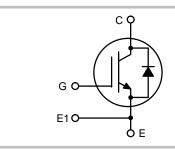
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

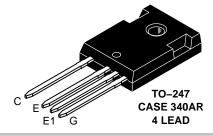


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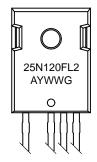
www.onsemi.com

25 A, 1200 V V<sub>CEsat</sub> = 2.0 V E<sub>on</sub> = 0.99 mJ





### MARKING DIAGRAM



25N120FL2 = Specific Device Code

A = Assembly Location

Y = Year WW = Work Week G = Pb-Free Package

## **ORDERING INFORMATION**

Device	Package	Shipping
NGTB25N120FL2WAG	TO-247 (Pb-Free)	30 Units / Rail

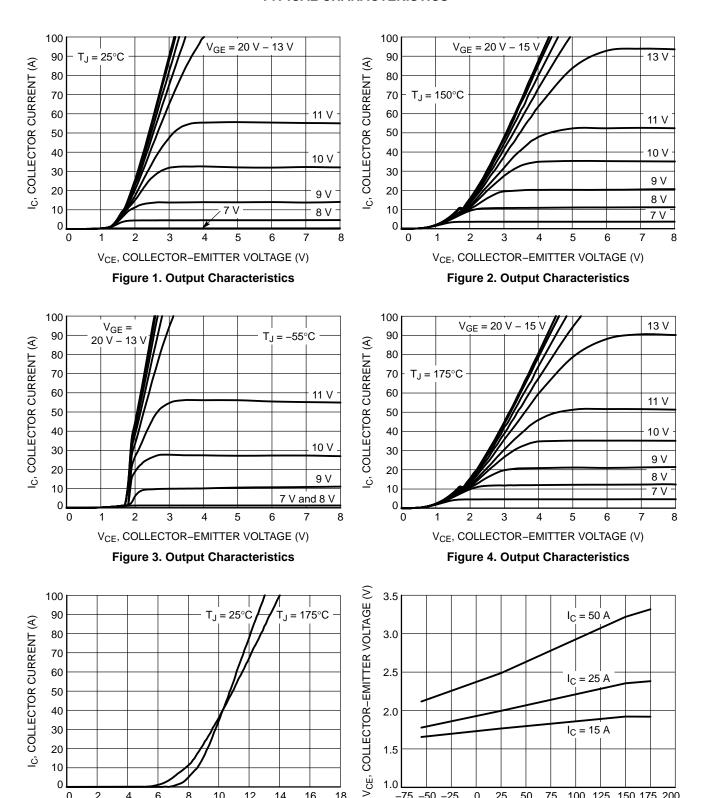
### THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal resistance junction–to–case, for IGBT	$R_{\theta JC}$	0.39	°C/W
Thermal resistance junction–to–case, for Diode	$R_{\theta JC}$	0.64	°C/W
Thermal resistance junction–to–ambient		25	°C/W

Parameter	Test Conditions	Symbol	Min	Тур	Max	Unit
STATIC CHARACTERISTIC	•					
Collector–emitter breakdown voltage, gate–emitter short–circuited	$V_{GE} = 0 \text{ V}, I_{C} = 500 \mu\text{A}$	V <sub>(BR)CES</sub>	1200	_	-	V
Collector-emitter saturation voltage	V <sub>GE</sub> = 15 V, I <sub>C</sub> = 25 A V <sub>GE</sub> = 15 V, I <sub>C</sub> = 25 A, T <sub>J</sub> = 175°C	V <sub>CEsat</sub>	_ _	2.00 2.40	2.40	V
Gate-emitter threshold voltage	$V_{GE} = V_{CE}, I_{C} = 400 \mu A$	V <sub>GE(th)</sub>	4.5	5.5	6.5	V
Collector-emitter cut-off current, gate- emitter short-circuited	V <sub>GE</sub> = 0 V, V <sub>CE</sub> = 1200 V V <sub>GE</sub> = 0 V, V <sub>CE</sub> = 1200 V, T <sub>J</sub> = 175°C	I <sub>CES</sub>	_ _	- 4.0	0.4	mA
Gate leakage current, collector-emitter short-circuited	V <sub>GE</sub> = 20 V , V <sub>CE</sub> = 0 V	I <sub>GES</sub>	-	-	200	nA
Input capacitance		C <sub>ies</sub>	_	4243	_	pF
Output capacitance	V <sub>CE</sub> = 20 V, V <sub>GE</sub> = 0 V, f = 1 MHz	C <sub>oes</sub>	_	159	_	
Reverse transfer capacitance	1 9-	C <sub>res</sub>	_	77	_	
Gate charge total		Qq	_	181	_	nC
Gate to emitter charge	V <sub>CE</sub> = 600 V, I <sub>C</sub> = 25 A, V <sub>GE</sub> = 15 V	Q <sub>ge</sub>	_	40	_	
Gate to collector charge		Q <sub>gc</sub>	_	87	_	
SWITCHING CHARACTERISTIC, INDUC	TIVE LOAD	<u>, J.</u>				
Turn-on delay time		t <sub>d(on)</sub>	_	17	_	ns
Rise time	1	t <sub>r</sub>	_	19	_	
Turn-off delay time	T <sub>J</sub> = 25°C	t <sub>d(off)</sub>	_	113	_	
Fall time	$V_{CC} = 600 \text{ V}, I_C = 50 \text{ A}$	t <sub>f</sub>	-	118	-	
Turn-on switching loss	$R_g = 10 \Omega$ $V_{GE} = \pm 15V$	E <sub>on</sub>	-	0.99	-	mJ
Turn-off switching loss	1	E <sub>off</sub>	-	0.66	-	
Total switching loss	1	E <sub>ts</sub>	-	1.65	-	1
Turn-on delay time		t <sub>d(on)</sub>	-	15	-	ns
Rise time	7	t <sub>r</sub>	-	19	-	
Turn-off delay time	T <sub>J</sub> = 175°C	t <sub>d(off)</sub>	_	120	_	
Fall time	$V_{CC} = 600 \text{ V}, I_C = 50 \text{ A}$	t <sub>f</sub>	-	193	-	
Turn-on switching loss	$R_g = 10 \Omega$ $V_{GE} = \pm 15 V$	E <sub>on</sub>	_	1.2	_	mJ
Turn-off switching loss	7	E <sub>off</sub>	-	1.3	-	
Total switching loss	7	E <sub>ts</sub>	_	2.5	_	
DIODE CHARACTERISTIC						
Forward voltage	$V_{GE} = 0 \text{ V, } I_F = 25 \text{ A}$ $V_{GE} = 0 \text{ V, } I_F = 25 \text{ A, } T_J = 175^{\circ}\text{C}$	V <sub>F</sub>	_ _	2.51 2.60	3.00	V
Reverse recovery time	T <sub>J</sub> = 25°C	t <sub>rr</sub>	-	136	-	ns
Reverse recovery charge	$I_F = 25 \text{ Å}, V_R = 400 \text{ V}$ $di_F/dt = 250 \text{ A/}\mu\text{s}$	Q <sub>rr</sub>	-	0.6	_	μC
Reverse recovery current	]	I <sub>rrm</sub>	-	8.4	-	Α
Reverse recovery time	T <sub>J</sub> = 175°C	t <sub>rr</sub>	-	251	-	ns
Reverse recovery charge	$I_F = 25 \text{ A}, V_R = 400 \text{ V}$ $di_F/dt = 250 \text{ A/}\mu\text{s}$	Q <sub>rr</sub>	-	1.91	-	μC
Reverse recovery current		I <sub>rrm</sub>	_	14	_	Α

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### TYPICAL CHARACTERISTICS



V<sub>GE</sub>, GATE-EMITTER VOLTAGE (V) **Figure 5. Typical Transfer Characteristics** 

10

12

16

18

-75 -50 -25

8

10

0

2

T<sub>J</sub>, JUNCTION TEMPERATURE (°C) Figure 6. V<sub>CE(sat)</sub> vs. T<sub>J</sub>

75 100 125 150 175 200

25 50

#### **TYPICAL CHARACTERISTICS**

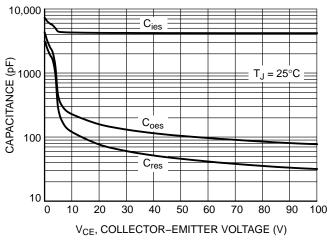


Figure 7. Typical Capacitance

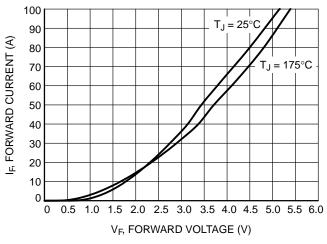


Figure 8. Diode Forward Characteristics

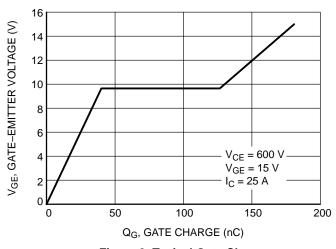


Figure 9. Typical Gate Charge

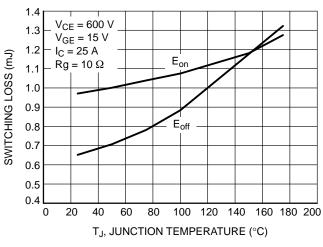


Figure 10. Switching Loss vs. Temperature

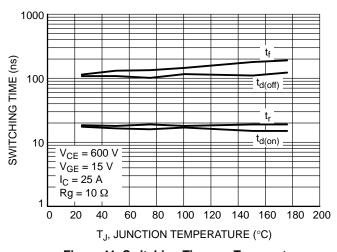


Figure 11. Switching Time vs. Temperature

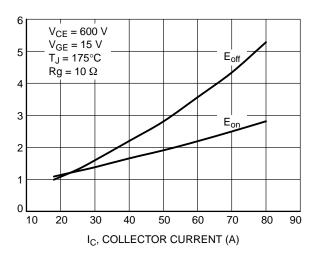


Figure 12. Switching Loss vs. IC

SWITCHING LOSS (mJ)

#### **TYPICAL CHARACTERISTICS**

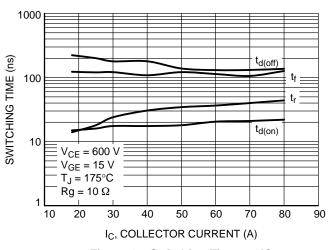


Figure 13. Switching Time vs. IC

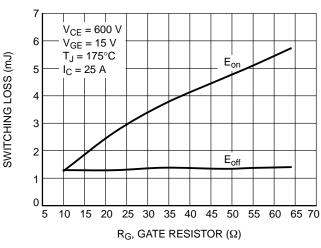


Figure 14. Switching Loss vs. RG

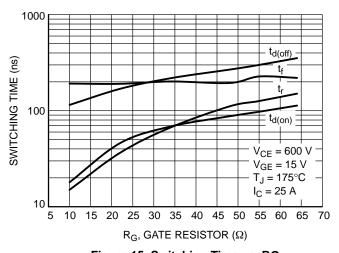


Figure 15. Switching Time vs. RG

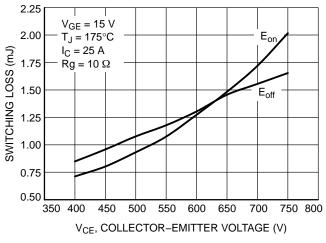


Figure 16. Switching Loss vs. V<sub>CE</sub>

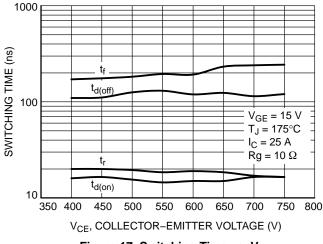


Figure 17. Switching Time vs. V<sub>CE</sub>

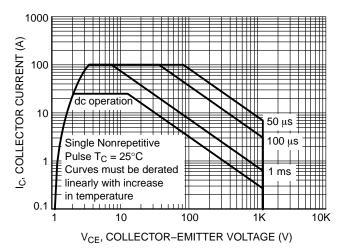


Figure 18. Safe Operating Area

#### **TYPICAL CHARACTERISTICS**

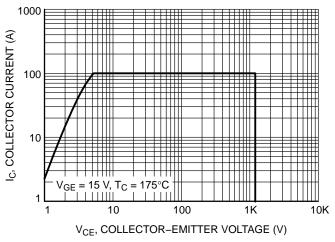


Figure 19. Reverse Bias Safe Operating Area

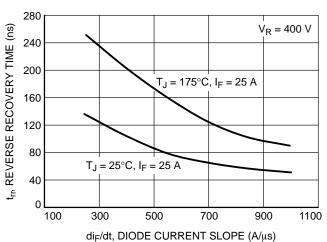


Figure 20. t<sub>rr</sub> vs. di<sub>F</sub>/dt

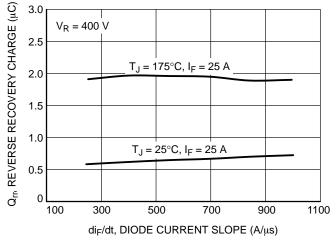


Figure 21. Q<sub>rr</sub> vs. di<sub>F</sub>/dt

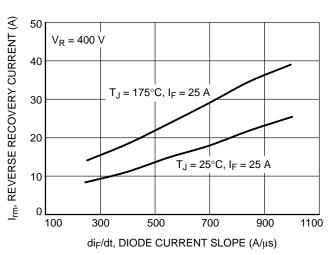


Figure 22. I<sub>rm</sub> vs. di<sub>F</sub>/dt

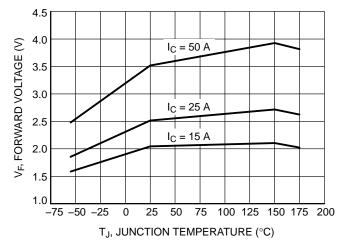


Figure 23. V<sub>F</sub> vs. T<sub>J</sub>

#### **TYPICAL CHARACTERISTICS**

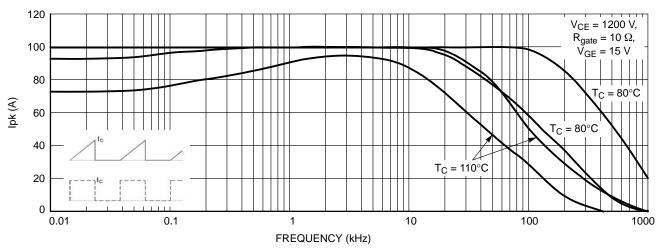


Figure 24. Collector Current vs. Switching Frequency

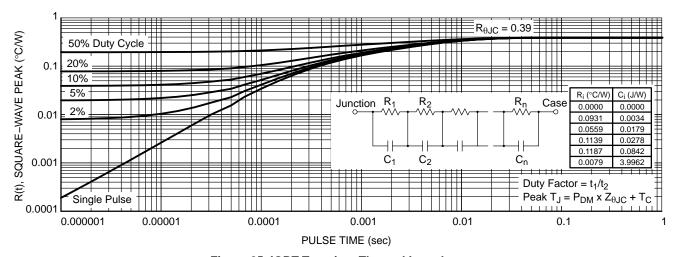


Figure 25. IGBT Transient Thermal Impedance

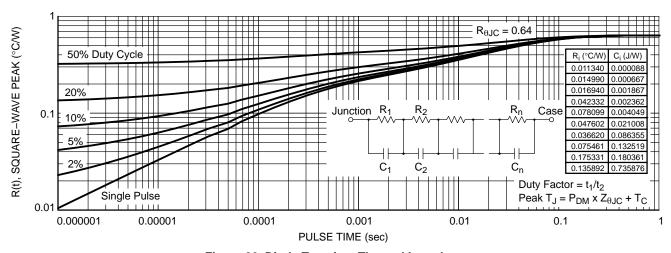


Figure 26. Diode Transient Thermal Impedance

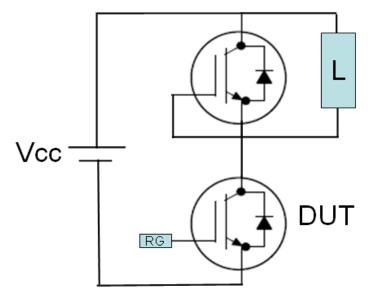


Figure 27. Test Circuit for Switching Characteristics

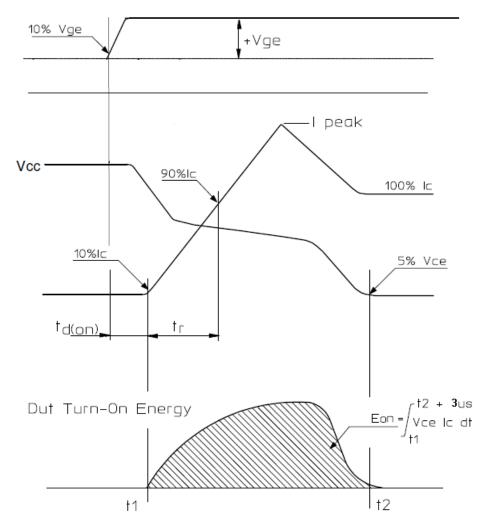


Figure 28. Definition of Turn On Waveform

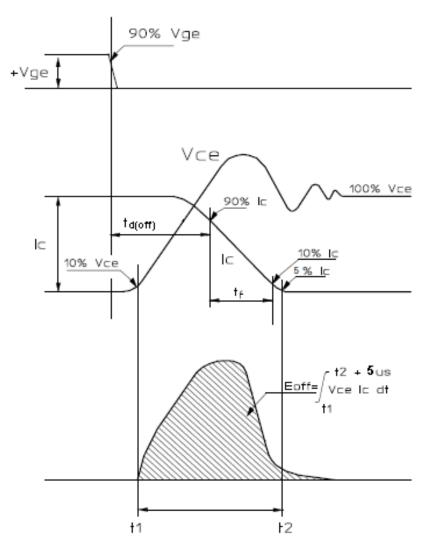
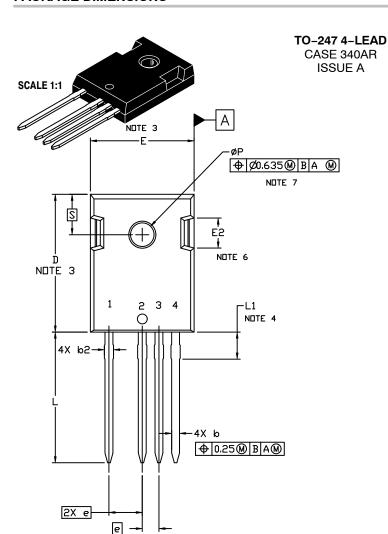
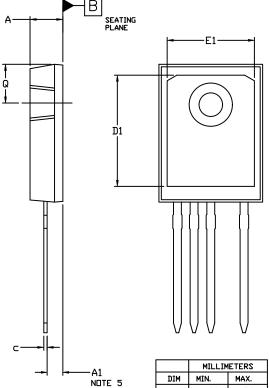


Figure 29. Definition of Turn Off Waveform



**DATE 07 MAY 2020** 

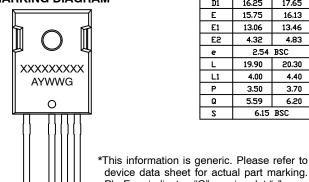


#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETER
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE DUTERMOST EXTREME OF THE PLASTIC BODY.
- 4. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.
- DIMENSION AT TO BE MEASURED IN THE REGION DEFINED BY L1.
- NOTCHES ARE REQUIRED BUT THEIR SHAPE IS OPTIONAL.
- 7. DIAMETER P SHALL HAVE A MAXIMUM DRAFT ANGLE OF 3.5° TO THE TOP OF THE PART WITH A MAXIMUM DIAMETER OF 4.20.

98AON97044F

#### **GENERIC MARKING DIAGRAM\***



Α	4.83	5.21	
A1	2.29	2.54	
b	1.10	1.30	
b2	1.30	1.50	
U	0.50	0.70	
D	20.80	21.10	
D1	16.25	17.65	
Ε	15.75	16.13	
E1	13.06	13.46	
E2	4.32	4.83	
6	2.54 BSC		
٦	19.90	20.30	
L1	4.00	4.40	
Р	3.50	3.70	
Q	5.59	6.20	
S	6.15 BSC		

XXXXX = Specific Device Code = Assembly Location

= Year WW = Work Week G = Pb-Free Package

or may not be present. Some products may not follow the Generic Marking. Electronic versions are uncontrolled except when accessed directly from the Document Repository.

device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "■", may

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