TDA38840 OptiMOS™ IPOL

40 A single-voltage synchronous Buck regulator

Features

- Single 4.3 V to 17 V application or Wide Input Voltage Range from 2.0 V to 17 V with an External VCC
- Precision Reference Voltage (0.6 V +/- 0.5%)
- Enhanced Fast COT Engine Stable with Ceramic Output Capacitors
- Optional Forced Continuous Conduction Mode and Diode Emulation for Enhanced Light Load Efficiency
- Programmable Switching Frequency from 600 kHz to 2 MHz
- Monotonic Start-Up with Four Selectable Soft-Start Times & Enhanced Pre-Bias Start-Up
- Thermally Compensated Internal Over Current Protection with Four Selectable Settings
- Enable input with Voltage Monitoring Capability & Power Good Output
- Thermal Shut Down
- Operating Temp: -40 °C $< T_j <$ 125 °C
- Small Size: 5 mm x 6 mm PQFN
- Halogen-free and RoHS2 Compliant with Exemption 7a

Potential applications

- Server Applications
- Storage Applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

The TDA38840 is an easy-to-use, fully integrated dc - dc Buck regulator. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make TDA38840 a small footprint solution, providing high-efficiency power delivery. Furthermore, it uses a fast Constant On-Time (COT) control scheme, which simplifies design efforts and achieves fast control response.

The TDA38840 has an internal low dropout voltage regulator, allowing operation with a single supply. It can also operate with an external bias supply, with an extended operating input voltage (PVin) range from 2.0 V to 17 V.

The TDA38840 is a versatile regulator, offering programmable switching frequency from 600 kHz to 2 MHz, four selectable current limits, four selectable soft-start times, Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DEM) operation.

It also features important protection functions, such as pre-bias start-up, thermally compensated current limit, over voltage and under voltage protection, and thermal shutdown to give required system level security in the event of fault conditions.

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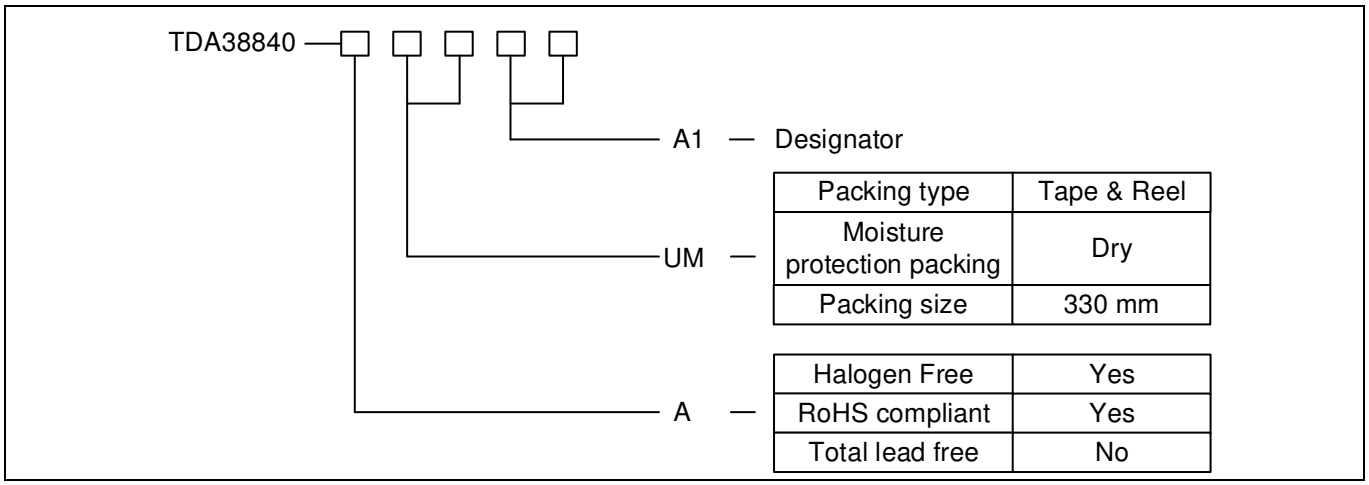
1 Ordering information

1. Ordering Information

Sales Product Number	Package Type	Standard Pack Form and Qty		Orderable Part Number
TDA38840	QFN 5 mm x 6 mm	Tape and Reel	5000	TDA38840AUMA1



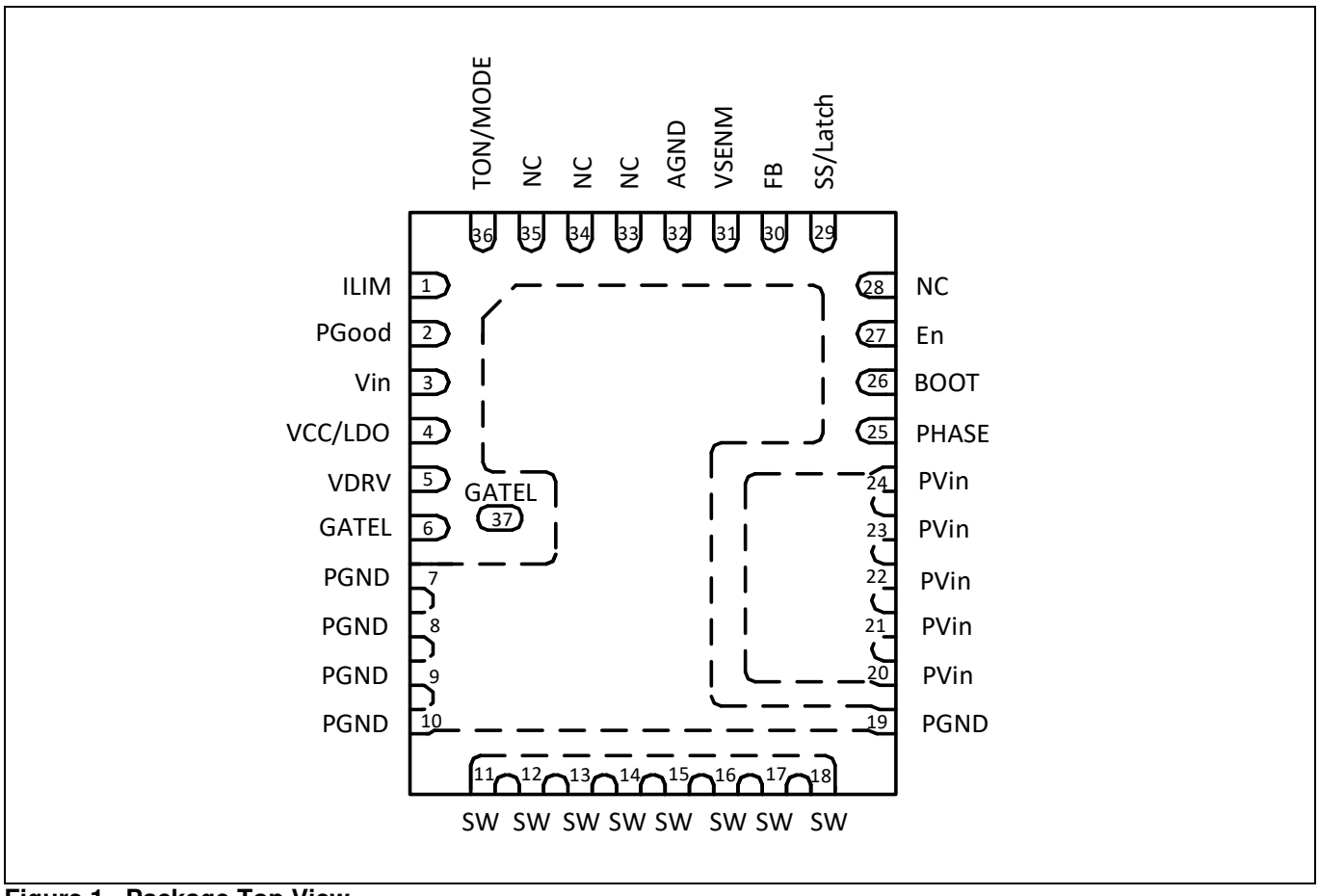


Figure 1 Package Top View

2 Functional block diagram

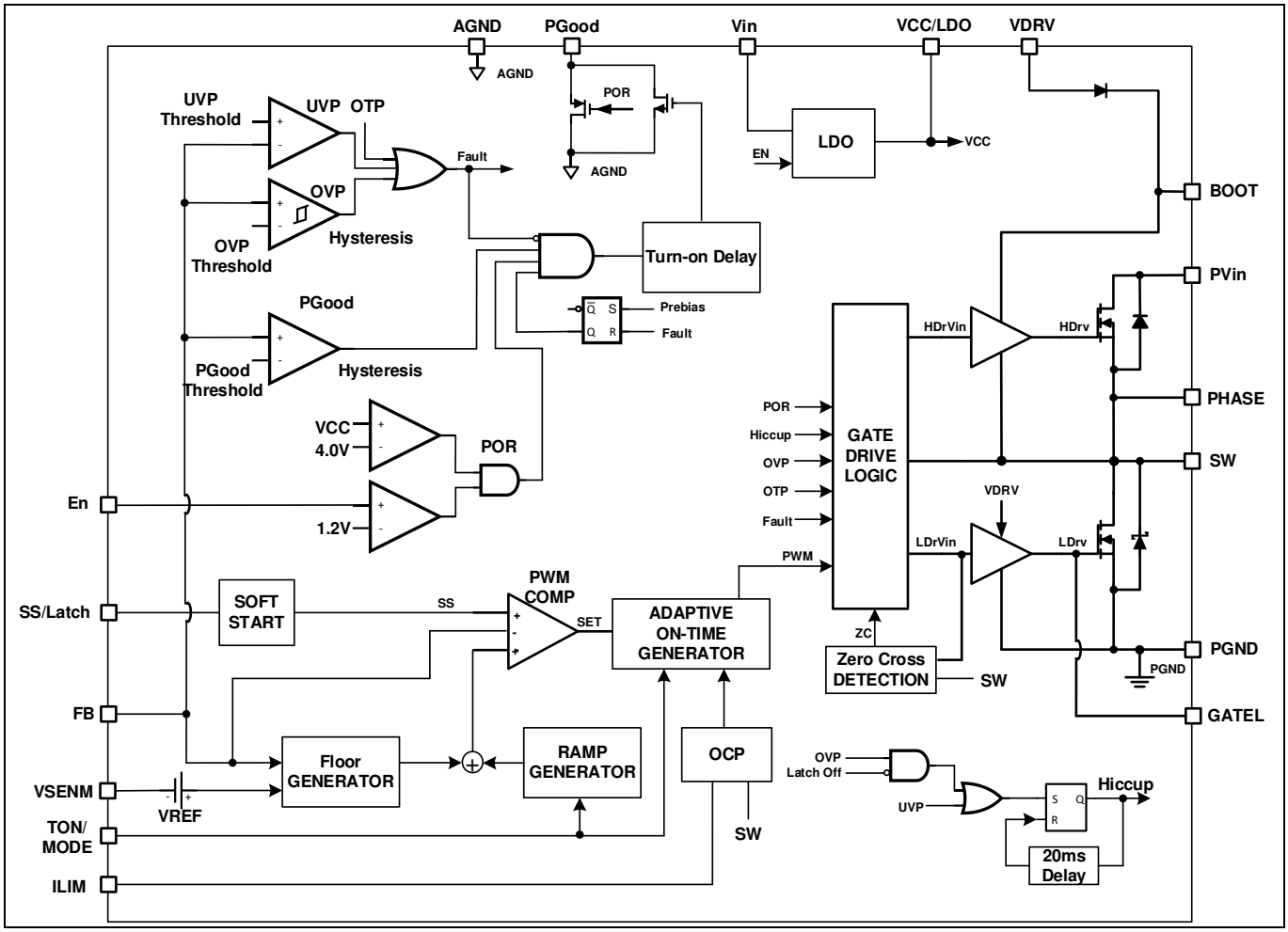


Figure 2 Block diagram

3 Typical application diagram

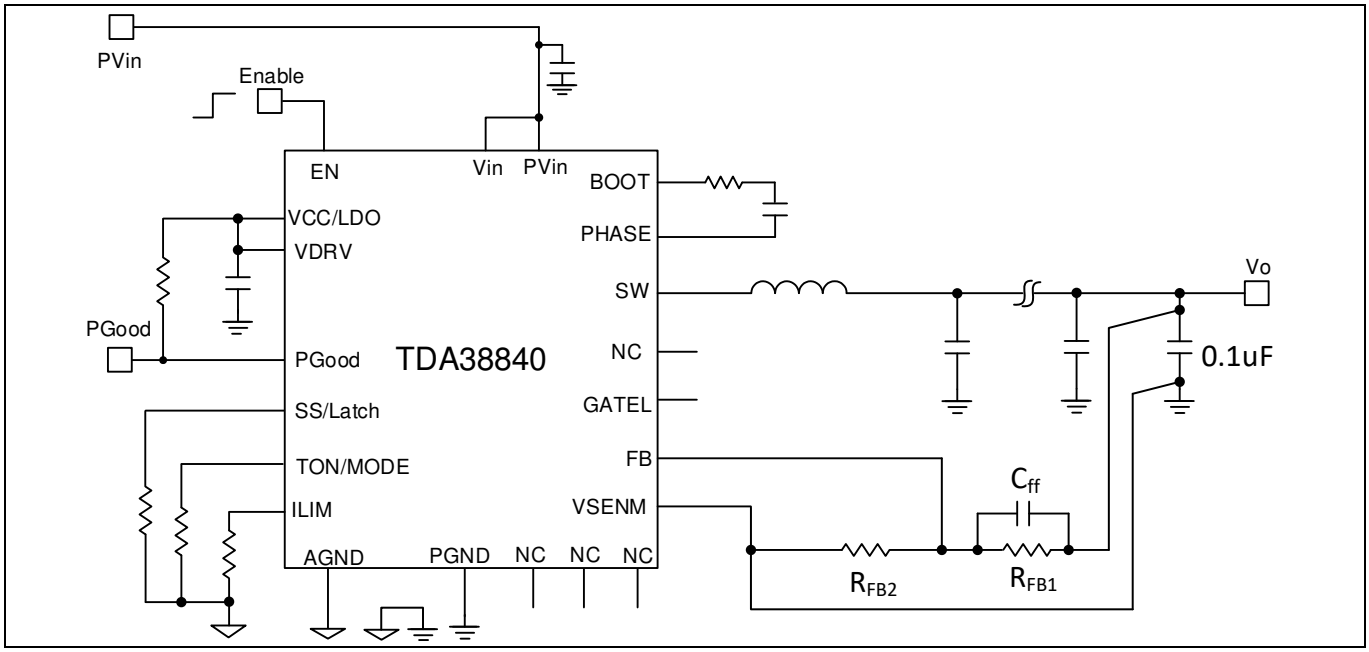


Figure 3 TDA38840 typical application circuit

4 Pin descriptions

Note: *I = Input, O = Output*

Pin#	Pin Name	I/O	Type	Pin Description
1	ILIM	I	Analog	Connect a resistor to a quiet ground to set the Over Current Protection (OCP) limit. Four user selectable OCP limits are available.
2	PGood	O	Analog	Power Good status output pin is open drain. Connect a pull up resistor from this pin to VCC or to an external bias voltage, e.g. a 50 kΩ pull-up resistor for a PGood bias voltage of 3.3 V.
3	Vin	I	Power	Input voltage for an Internal LDO. A 4.7 µF capacitor should be connected between this pin and PGND. If an external supply is connected to VCC/LDO pin, this pin should be shorted to VCC/LDO pin and a 10 µF ceramic capacitor can be shared with Vin and VCC/LDO pin.
4	VCC/LDO	I/O	Power	Output of the internal LDO or input for an external VCC voltage. A 2.2 µF - 10 µF ceramic capacitor is recommended to use between VCC, VDRV and the Power ground (PGND).
5	VDRV	I	Power	Input bias for the internal driver. It should be shorted to VCC/LDO pin on the PCB. A 2.2 µF - 10 µF ceramic capacitor is recommended to use between VDRV, VCC/LDO and the Power ground (PGND).
6, 37	GATEL	I	Analog	Gate of Low-side FET. This pin can be used to monitor the gate signal of LS FET. No external components should be connected to it.
7, 8, 9, 10, 19	PGND	-	Ground	Power Ground. Must be connected to the system's power ground plane. PGND and AGND are internally connected via the lead frame.
11, 12, 13, 14, 15, 16, 17, 18	SW	O	Power	Switch Node. Connect these pins to an output inductor.
20, 21, 22, 23, 24	PVin	I	Power	Input supply for the power stage.
25	PHASE	O	Analog	Source of High-side FET. Connect a bootstrap capacitor between this pin and BOOT pin. A high temperature (X7R) 0.1 µF or greater value ceramic capacitor is recommended.
26	BOOT	I	Analog	Supply voltage for the high side driver. Connect this pin to the PHASE pin through a bootstrap capacitor. A resistor (e.g., 1 Ω~2 Ω) can be placed in series with the bootstrap capacitor to control the slew rate of the SW node rising edge.
27	En	I	Analog	Multi-function pin: (1) Enable pin to turn the device on and off; (2) enable or disable the internal LDO; (3) If this pin is connected to PVin pin through a resistor divider, input voltage UVLO can be implemented.

Pin#	Pin Name	I/O	Type	Pin Description
29	SS/Latch	I	Analog	Multi-function pin. Connect a resistor to a quiet ground to select Soft-Start time from 4 options. This pin also selects latched-off Over Voltage Protection (OVP) or non-latched OVP.
30	FB	I	Analog	Output voltage feedback pin. Connect this pin to the output of the regulator via a resistor divider to set the output voltage.
31	VSENM	-	Analog	This pin provides the return connection for a pseudo remote voltage sensing. The feedback resistor divider should be connected to this pin. It is also used as ground for the internal reference voltage.
32	AGND	-	Ground	Signal ground for the internal circuitry except the internal reference voltage.
36	TON/MODE	I	Analog	Multi-function pin. Connect a resistor to a quiet ground to set the switching frequency to 1 of 8 settings and sets the mode of operation to FCCM or DEM.
28, 33, 34, 35	NC	-	Not connected	Not connected internally. They can be left floating on PCB.

5 Absolute maximum ratings

Absolute maximum ratings

Description	Min	Max	Unit	Conditions
PVin, Vin and En to PGND	-0.3	25	V	Note **1**
PVin to SW and PHASE	-0.3 V(dc) , below -5 V for 5 ns	25 V(dc), above 32 V for 2 ns	V	
VCC and VDRV to PGND	-0.3	6	V	Note **1**
BOOT to PGND	-0.3 V(dc), below -0.3 V for 5 ns	29	V	Note **1**
SW and PHASE to PGND	-0.3 (dc), below -5 V for 5 ns	25 V(dc), above 32 V for 2 ns	V	Note **1**
BOOT to PHASE	-0.3	6 V(dc), 7 V for 5 ns	V	
ILIM, FB, PGood, TON/MODE, GATEL and SS to AGND	-0.3	6	V	Note **1**
PGND to AGND	-0.3	0.3	V	
VSENM to AGND	-0.3	0.3	V	
Storage Temperature Range	-55	150	°C	
Junction Temperature Range	-40	150	°C	

Note:

1. PGND, VSENM, and AGND pin are connected together

Attention: ***Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

6 Thermal Characteristics

6.1 Thermal Characteristics

Description	Symbol	Values	Test Conditions
Junction to Ambient Thermal Resistance	θ_{JA}	12 °C/W	Note **2**
Junction to PCB Thermal Resistance	$\theta_{JC\text{-}PCB}$	0.85 °C/W	Note **3**
Junction to Case Top Thermal Resistance	θ_{JC}	22.5 °C/W	

Note:

2. *Thermal resistance is measured with components mounted on a standard EVAL_38840_1Vout demo board in free air.*
3. *Thermal resistance is based on the board temperature near pin 22.*

7 Electrical specifications

7.1 Recommended operating conditions

Description	Min	Max	Unit	Note
PVin Voltage Range with External VCC	2	17	V	Note **4**, Note **5**
PVin Voltage Range with Internal LDO	4.5	17	V	Note **5**, Note **6 & 10**
VCC and VDRV Supply Voltage Range	4.3	5.5	V	Note **4**, Note **7**
Typical Output Voltage Range	0.6	6	V	Note **8**, Note **9**
Continuous Output Current Range		40	A	Note **9**
Typical Switching Frequency Range	600	2000	kHz	Note **10**
Operating Junction Temperature	-40	125	°C	

Note:

4. *Vin is shorted to VCC and uses an external bias voltage.*
5. *A common practice is to have 20% margin on the maximum SW node voltage in the design. To ensure the maximum SW node spike voltage does not exceed 20 V, a small resistor in series with the Boot pin might be needed. Alternatively, a RC snubber can be used at the SW node to reduce the SW node spike.*
6. *Vin is connected to PVin and the internal LDO is used. For single-rail applications with the internal LDO and PVin =Vin = 4.3 V-5.4 V, the internal LDO may enter dropout mode. OCP limits can be reduced due to the lower VCC voltage. Please refer to **Section 12.7** for more detailed design guidelines.*
7. *The TDA38840 is designed to function with VCC down to 4.2 V, however, electrical specifications such as OCP limits may be degraded.*
8. *The maximum output voltage is also limited by the minimum off-time. Please refer to **Section 12.13** for details. Also note that OCP limit may be degraded when off-time is close to the minimum off-time.*
9. *Refer to **Section 9** for maximum output current rating at different ambient temperatures using internal LDO. Lower VCC voltage can result in higher $R_{DS(on)}$ and therefore require more thermal derating.*
10. *The maximum LDO output current must be limited within 50 mA for operations requiring full operating temperature range of -40 °C ≤ T_J ≤ 125 °C. **Figure 6** shows the maximum LDO output current capability over junction temperature. Thermal de-rating may be needed at an elevated ambient temperature to ensure the junction temperature remains within the recommended operating range.*

7.2 Electrical characteristics

Note: Unless otherwise specified, the specifications apply over 4.5 V ≤ Vin = PVin ≤ 17 V, 0 °C < T_J < 125 °C. Typical values are specified at Ta = 25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Top Switch	$R_{ds(on)\_Top}$	V_{Boot} – V_{sw}= 5.0 V, I_O = 40 A, T_j=25 °C		2.4		mΩ
Bottom Switch	$R_{ds(on)\_Bot}$	VCC = 5.0 V, Io = 40 A, T_j =25 °C		0.8		mΩ
Bootstrap Forward Voltage		I(BOOT) = 25 mA		378	600	mV
SW float voltage	V_{SW}	En = 0 V			300	mV
		En = high, No Switching			300	mV
Dead Band Time	T_{db}	SW node falling edge, Io = 40 A, Internal LDO, T_j = 25 °C, Note **11**		10		ns
		SW node rising edge, Io = 40 A, Internal LDO, T_j = 25 °C, Note **11**		5		ns
Supply Current						
Vin Supply Current (standby)	$I_{in(Standby)}$	En = Low, No Switching		4	10	µA
Vin Supply Current (static)	$I_{in(Static)}$	En=2 V, No Switching		2.3	4	mA
Soft Start						
Soft Start Ramp Rate	SS rate	SS/Latch = 0 kΩ, 4.53 kΩ, 10.5 kΩ, 18.7 kΩ;	0.4	0.6	0.84	mV/µs
		SS/Latch =1.5 kΩ, 5.76 kΩ, 12.1 kΩ, 21.5 kΩ;	0.2	0.3	0.42	mV/µs
		SS/Latch = 2.49 kΩ, 7.32 kΩ, 14 kΩ, 24.9 kΩ, Floating	0.1	0.15	0.21	mV/µs
		SS/Latch = 3.48 kΩ, 8.87 kΩ, 16.2 kΩ, 28.7 kΩ;	0.05	0.075	0.105	mV/µs
Feedback Voltage						
Feedback Voltage	V_{FB}			0.6		V
Accuracy		0°C < T_j < 85 °C	-0.5		+0.5	%
		-40 °C < T_j < 125 °C, Note **12**	-1		1	%
V_{FB} Input Current	IV_{FB}	V_{FB}=0.6 V, T_j=25 °C	-150	0	+150	nA
On-Time Timer Control						
On Time	T_{on}	Vin=12 V, Vo=1 V, TON= 0 kΩ or 10.5 kΩ, Note **13**		151		ns
		Vin=12 V, Vo=1 V, TON= 1.5 kΩ or 12.1 kΩ, Note **13**		114		ns
		Vin=12 V, Vo=1 V, TON= 2.49 kΩ, or 14 kΩ, Note **13**		91.5		ns
		Vin=12 V, Vo=1 V, TON= 3.48 kΩ, or 16.2 kΩ, Note **13**		77		ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
On Time	T_{on}	Vin=12 V, Vo=1 V, TON= 4.53 kΩ, or 18.7 kΩ, Note **13**		66.5		ns
		Vin=12 V, Vo=1 V, TON= 5.76 kΩ, or 21.5 kΩ, Note **13**		58.5		
		Vin=12 V, Vo=1 V, TON= 7.32 kΩ, or 24.9 kΩ, Note **13**		52		
		Vin=12V , Vo=1 V, TON= 8.87kΩ, or 28.7kΩ, Note **13**		47		
		Vin=12V, Vo=1.0V, TON = Floating, Note **13**		114		
Minimum On-Time	$T_{on\ (Min)}$	Vin=12 V, Vo=0 V		23	32	ns
Minimum Off-Time	$T_{off\ (Min)}$	T_j=25 °C, V_{FB}=0 V		270	360	ns
VCC LDO Output						
Output Voltage	VCC	5.5 V ≤ Vin ≤ 17 V, when Icc =50 mA, Cload = 2.2 µF	4.7	5.0	5.3	V
VCC Dropout	VCC_drop	Vin = 4.3 V, Icc=50 mA, Cload=2.2 µF			300	mV
Short Circuit Current	I_{short}	5.5 V ≤ Vin ≤ 17 V		90		mA
Under Voltage Lockout						
VCC-Start Threshold	VCC_UVLO_Start	VCC Rising Trip Level	3.8	4.0	4.2	V
VCC-Stop Threshold	VCC_UVLO_Stop	VCC Falling Trip Level	3.6	3.8	4.0	V
Enable-Start-Threshold	En_UVLO_Start	ramping up	1.14	1.2	1.36	V
Enable-Stop-Threshold	En_UVLO_Stop	ramping down	0.9	1	1.06	
Input Impedance	R_{EN}		500	1000	1500	kΩ
Over Current Limit						
Current Limit Threshold (Valley current)	Ioc	Tj = 25 °C, PVin = 12 V, Internal LDO, RILIM=24.9 kΩ, Note **14**	43	51	55	A
		Tj = 25 °C, PVin = 12 V, Internal LDO, RILIM=21.5 kΩ, Note **14**	38	44	48	
		Tj = 25 °C, PVin = 12 V, Internal LDO, RILIM=16.2 kΩ, Note **14**	32	38	41	
		Tj = 25 °C, PVin = 12 V, Internal LDO, RILIM=12.1 kΩ, Note **14**	26	31	34	
Over Voltage Protection						
OVP Trip Threshold	OVP_Vth	FB Rising	115	121	125	% Vref
		FB Falling, OVP hysteresis	110	115	120	
OVP Protection Delay	OVP_Tdly			8		µs
Hiccup Blanking Time	Tblk_Hiccup	Unlatched OVP		20		ms
Under Voltage Protection						
UVP Trip Threshold	UVP_Vth	FB Falling	65	70	75	% Vref
UVP Protection Delay	UVP_Tdly			2		µs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hiccup Blanking Time	Tblk_Hiccup			20		ms
Power Good						
PGood Turn on Threshold	VPG(upper)	FB Rising	85	91	95	% Vref
PGood Turn off Threshold	VPG(lower)	FB Falling	80	84	90	% Vref
PGood Sink Current	I_{PG}	PG = 0.5 V, En = 2 V	2.5	5		mA
PGood Voltage Low	$V_{PG(low)}$	Vin = VCC =0 V, Rpull-up = 50 kΩ to 3.3 V		0.3	0.5	V
PGood Turn on Delay	$V_{PG(on)\_Dly}$	FB Rising, see VPG(upper)		2.5		ms
PGood Comparator Delay	$V_{PG(comp)\_Dly}$	VFB < VPG(lower) or VFB > VPG(upper)	1	2	3.5	µs
PGood Open Drain Leakage Current		PG = 3.3 V			1	µA
Thermal Shutdown						
Thermal Shutdown		Note **11**		140		°C
Hysteresis		Note **11**		20		

Note:

11. Guaranteed by construction and not tested in production

12. Cold and hot temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

13. The Ton is trimmed so that the target switching frequency is achieved at around 30A load current using EVAL_38840_1Vout demo board.

*14. The specified OCP limits refer to the valley of the inductor current when OCP is tripped. For more detailed design guidelines, please refer to Section **12.8**.*

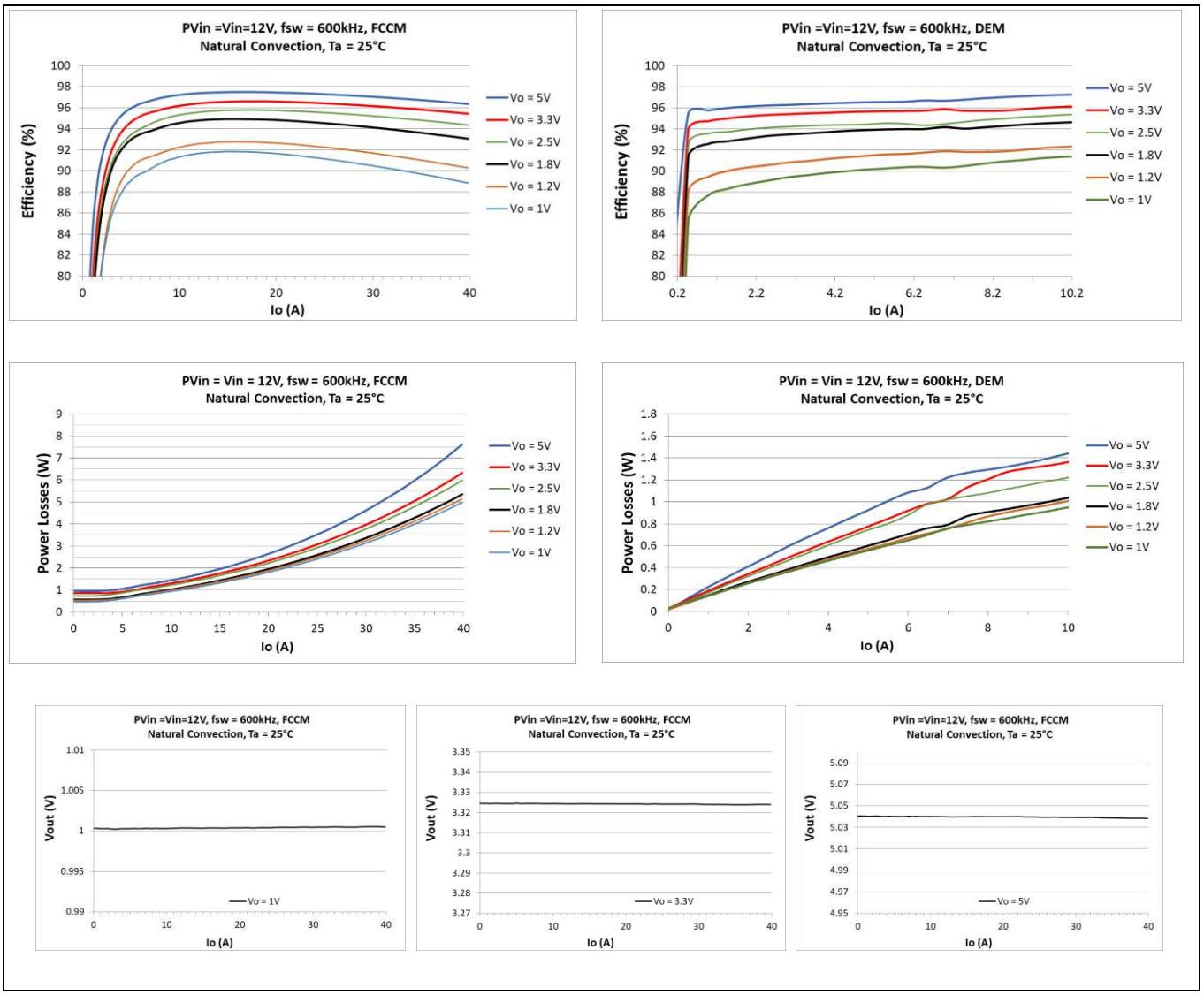
8 Typical efficiency and power loss curves

8.1 PVin = Vin = 12 V, fsw = 600 kHz

PVin = Vin = 12 V, VCC = Internal LDO, Io = 0 A-40 A, fsw= 600 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of TDA38840, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Table 1 Inductors for PVin = Vin = 12 V, fsw = 600 kHz

Vo (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
1.0	120	AH3740A-120K (ITG)	0.145	6.4x9.5x10
1.2	120	AH3740A-120K (ITG)	0.145	6.4x9.5x10
1.8	170	HCB138380F-171 (Delta)	0.15	12.4x8.3x8
2.5	250	HCUVE117512-251 (Delta)	0.15	7.5x10.7x12
3.3	250	HCUVE117512-251 (Delta)	0.15	7.5x10.7x12
5	350	HCBD101195-351(Delta)	0.35	10.1 x 11.4 x 9.5

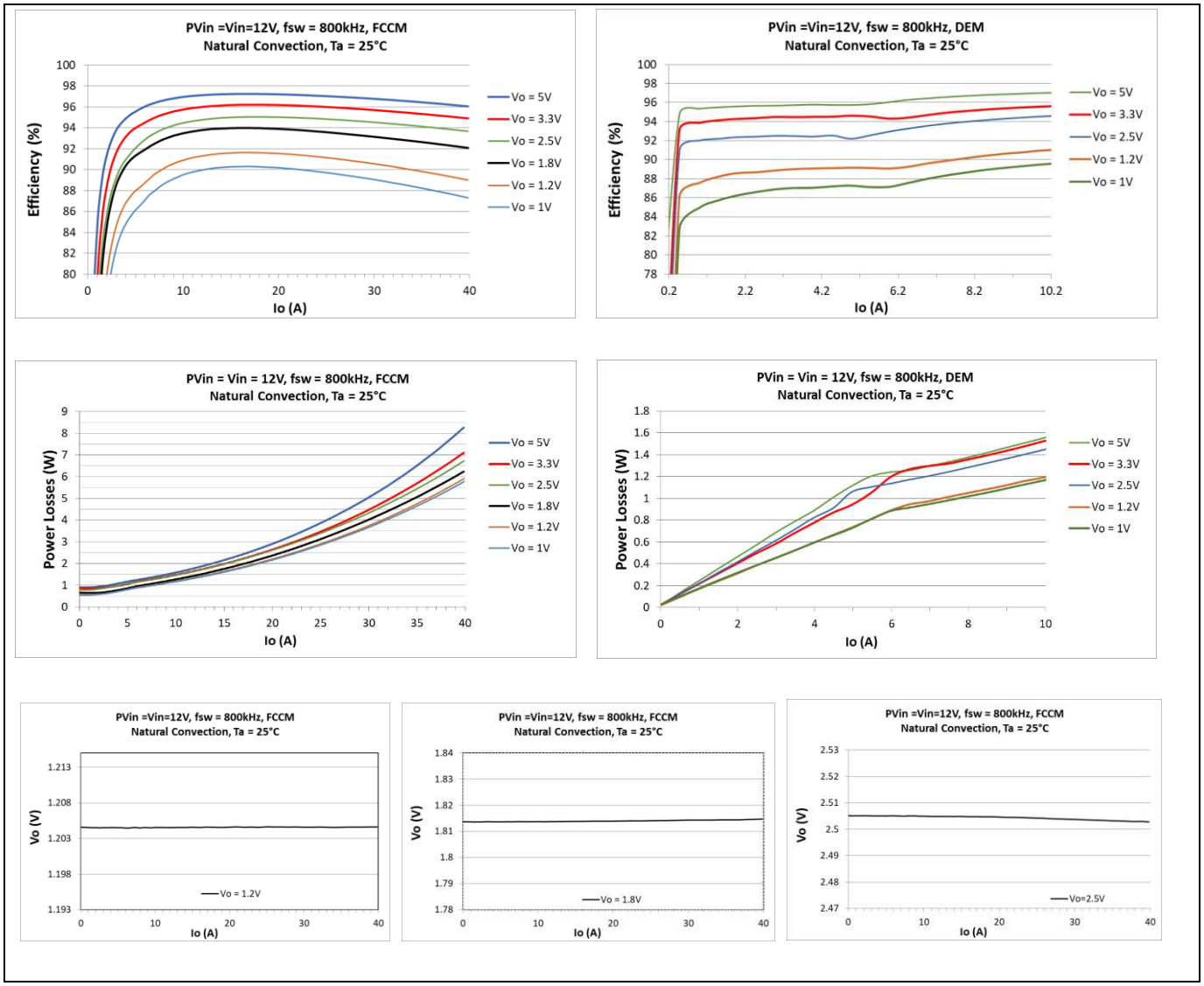


8.2 PVin = Vin = 12 V, fsw = 800 kHz

PVin = Vin = 12 V, VCC = Internal LDO, Io = 0 A-40 A, fsw = 800 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of TDA38840, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Table 2 Inductors for PVin = Vin =12 V, fsw = 800 kHz

Vo (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
1.0	100	HCBS9610W-101IF (Delta)	0.145	6.4 x 9.6 x 10
1.2	120	HCBS9610W-121IF (Delta)	0.15	6.4 x 9.6 x 10
1.8	150	HCB138380F-151 (Delta)	0.15	12.4 x 8.3 x 8
2.5	250	HCUVE117512-251 (Delta)	0.15	7.5x10.7x12
3.3	250	HCUVE117512-251 (Delta)	0.15	7.5x10.7x12
5	350	HCBD101195-351(Delta)	0.35	10.1 x 11.4 x 9.5

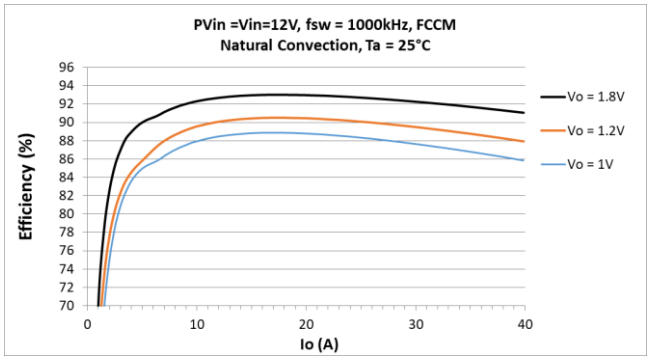


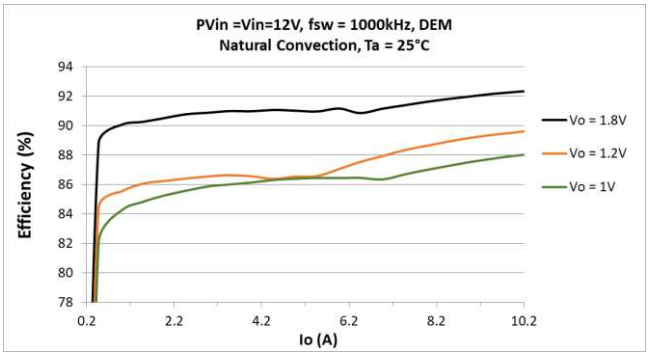
8.3 PVin = Vin = 12 V, fsw = 1000 kHz

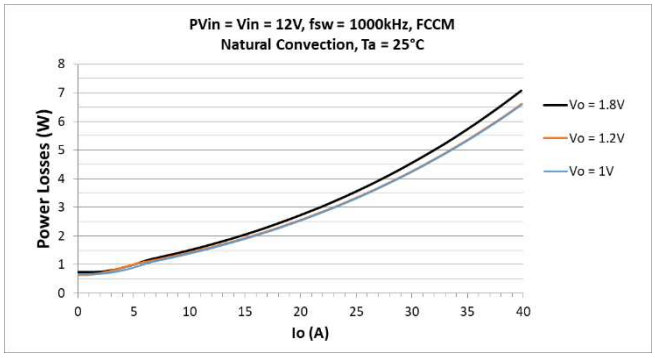
PVin = Vin = 12 V, VCC = Internal LDO, Io = 0 A-40 A, fsw = 1000 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of TDA38840, the inductor losses, the losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

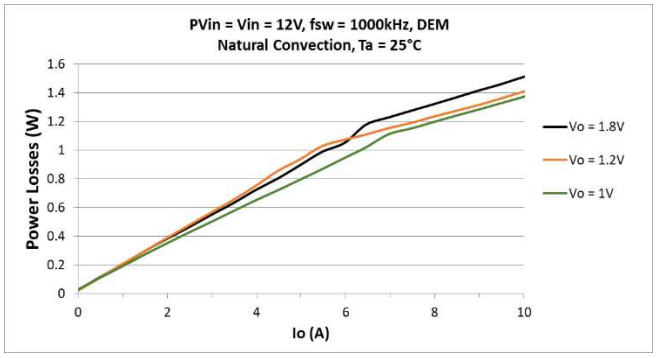
Table 3 Inductors for PVin = Vin = 12 V, fsw = 1000 kHz

Vo (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
1.0	100	AH3740A-70K (ITG)	0.145	6.4 x 9.5 x 10
1.2	100	AH3740A-100K (ITG)	0.145	6.4 x 9.5 x 10
1.8	120	AH3740A-120K (ITG)	0.145	6.4 x 9.5 x 10







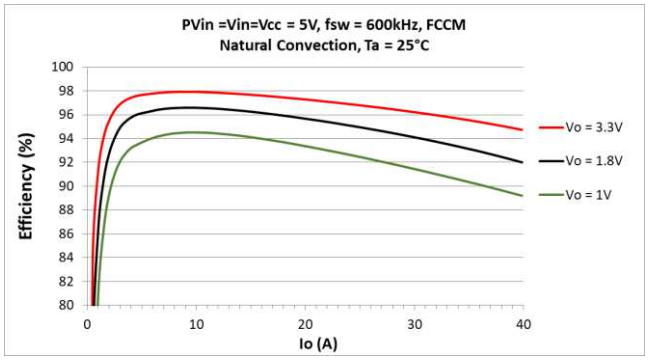


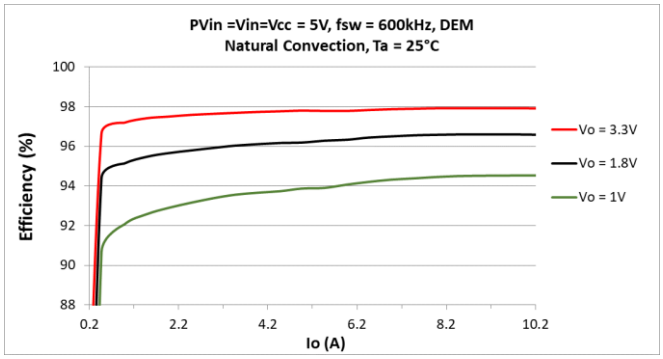
8.4 PVin = Vin = VCC = 5 V, fsw = 600 kHz

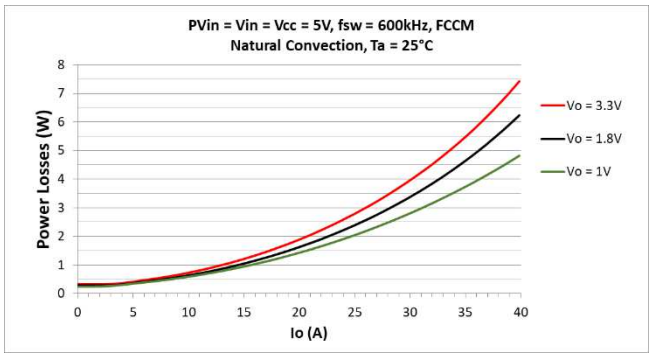
PVin = Vin = VCC = 5.0 V, Io = 0 A – 40 A, fsw = 600 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of TDA38840, the inductor losses, the losses of the input and output capacitors and and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

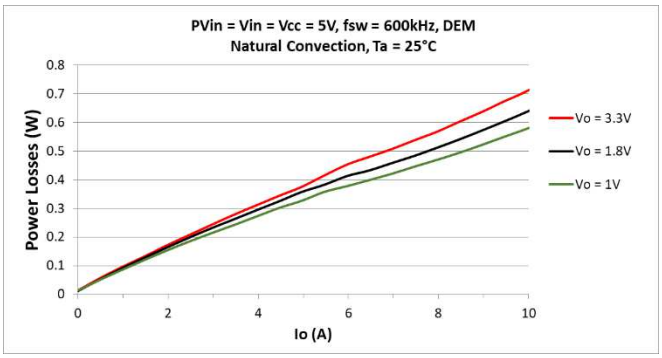
Table 4 Inductors for PVin = Vin = VCC= 5 V, fsw = 600 kHz

Vo (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
1.0	120	AH3740A-120K (ITG)	0.145	6.4 x 9.5 x 10
1.8	150	HCB138380F-151 (Delta)	0.15	12.4 x 8.3 x 8
3.3	150	HCB138380F-151 (Delta)	0.15	12.4 x 8.3 x 8



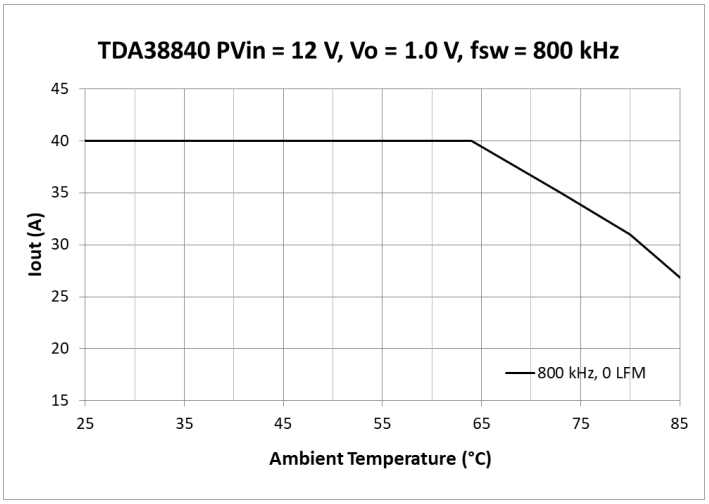


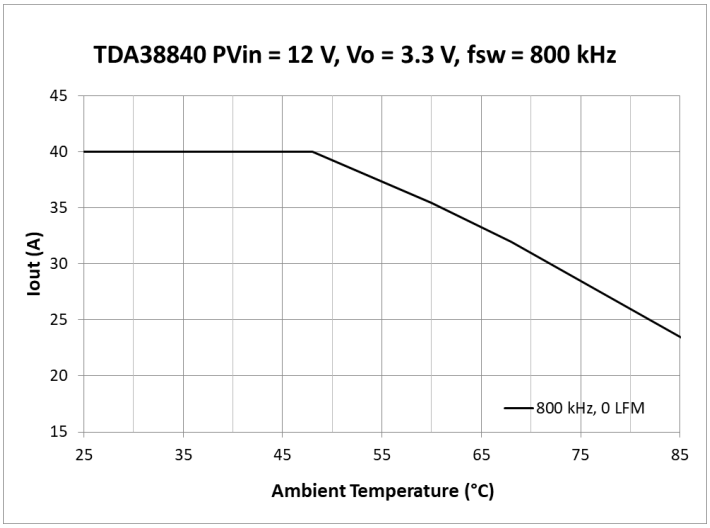




9 Thermal De-rating curves

Measurement is done on Evaluation board of EVAL_38840_1Vout. PCB is an 8-layer board with 2 ounce Copper for all layers, FR4 material, size 3.3”x4.05”.





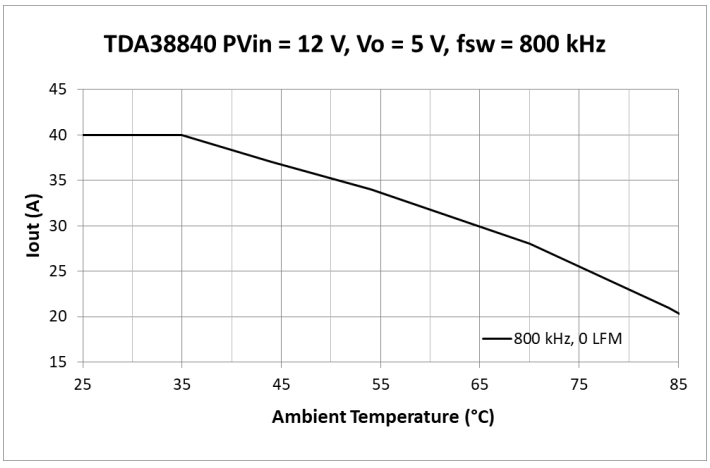
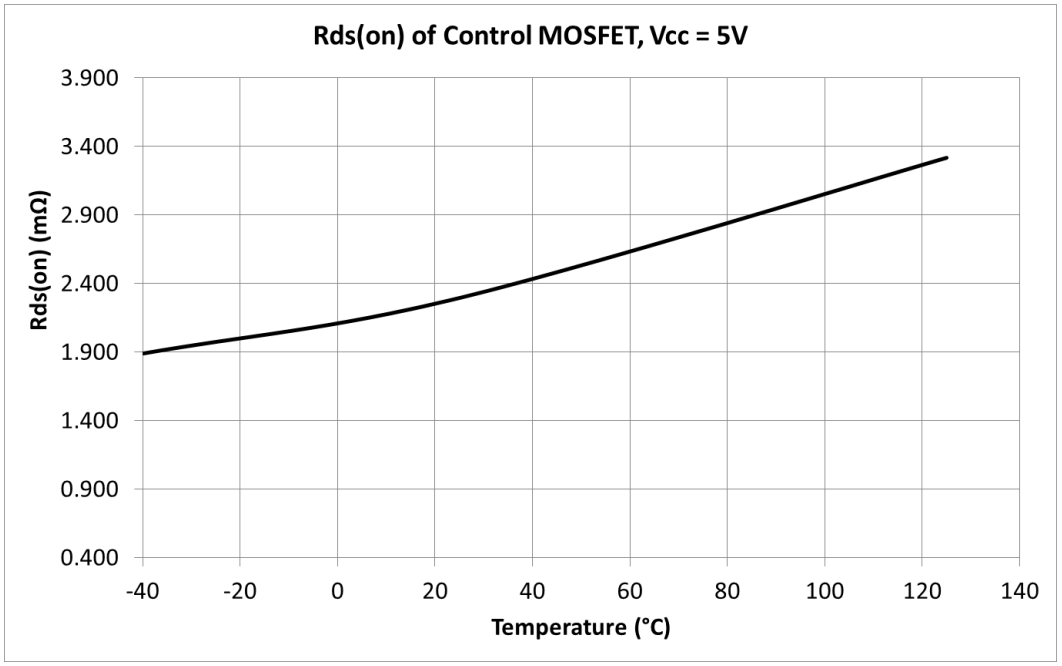


Figure 4 Thermal de-rating curves, PVin = 12 V, Vo = 1.0 V/3.3 V/5 V, Fsw = 800 kHz, VCC = Internal LDO

10 $R_{DS(ON)}$ of MOSFET Over Temperature



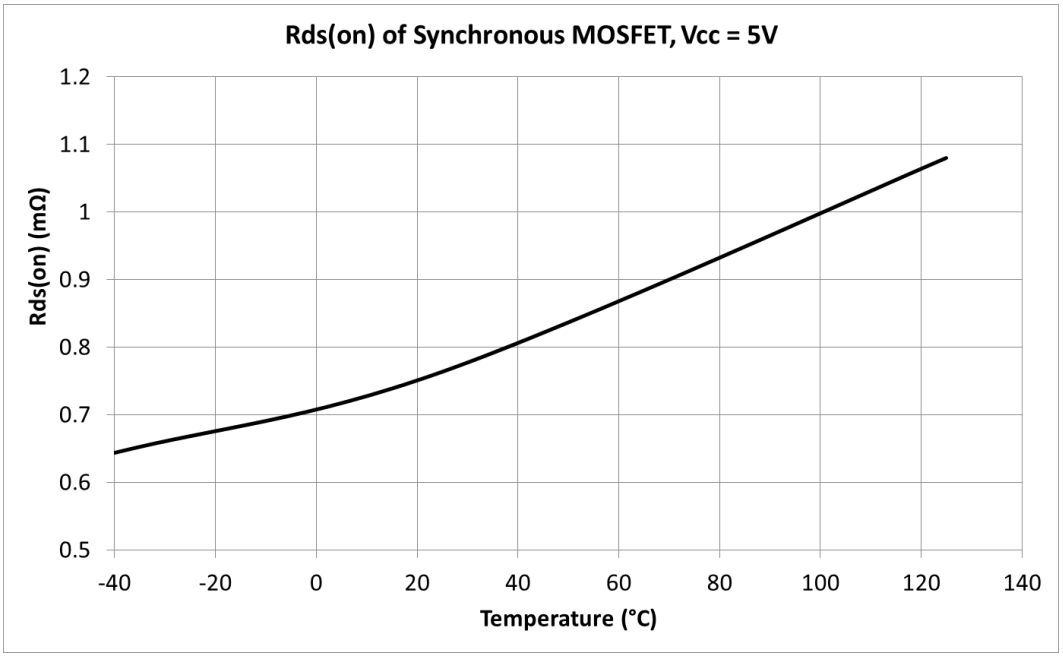


Figure 5 $R_{DS(on)}$ of MOSFETs over Junction Temperature

11 Typical operating characteristics (-40 °C ≤ T_j ≤ +125 °C)

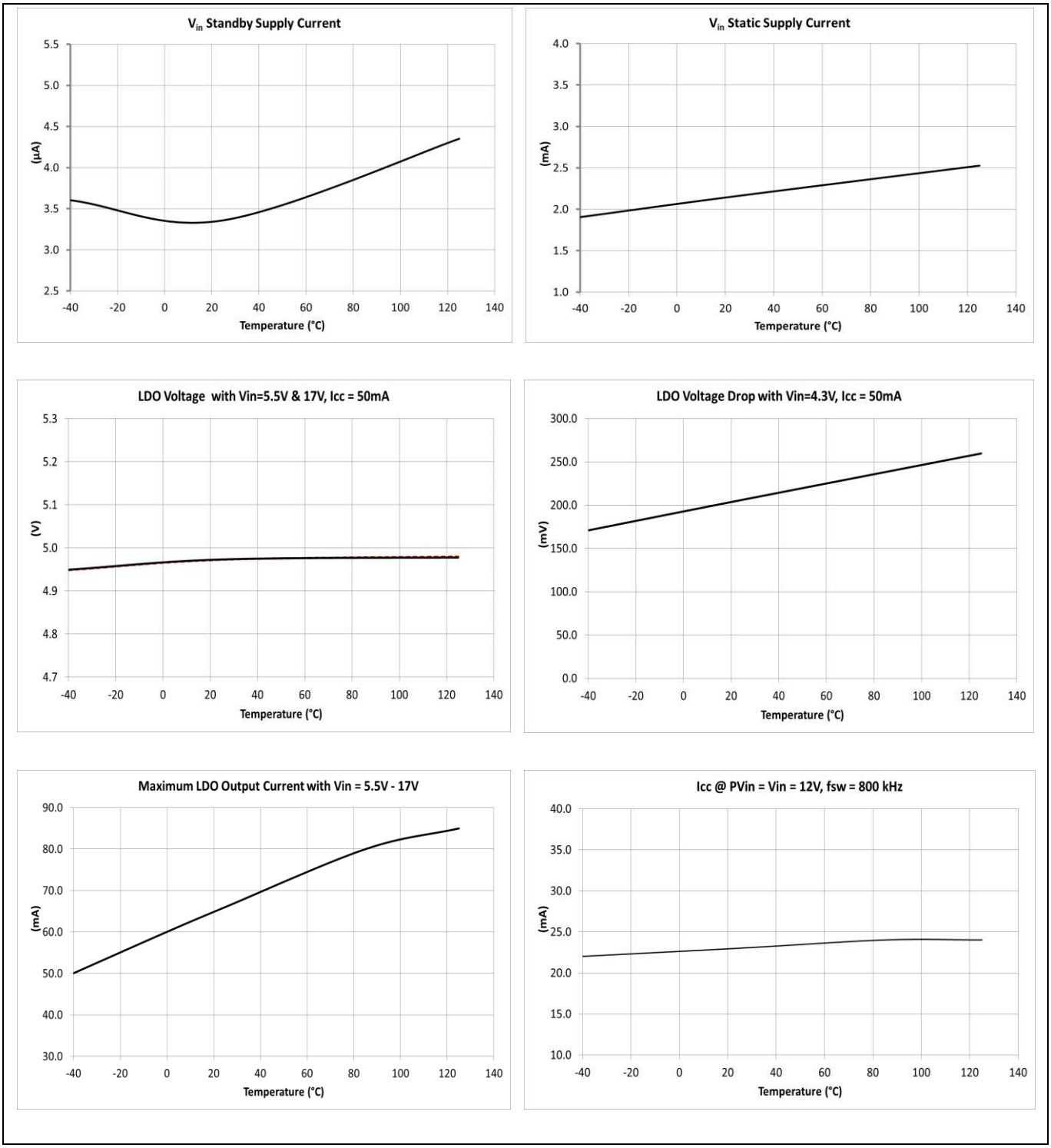


Figure 6 Typical operating characteristics (set 1 of 3)

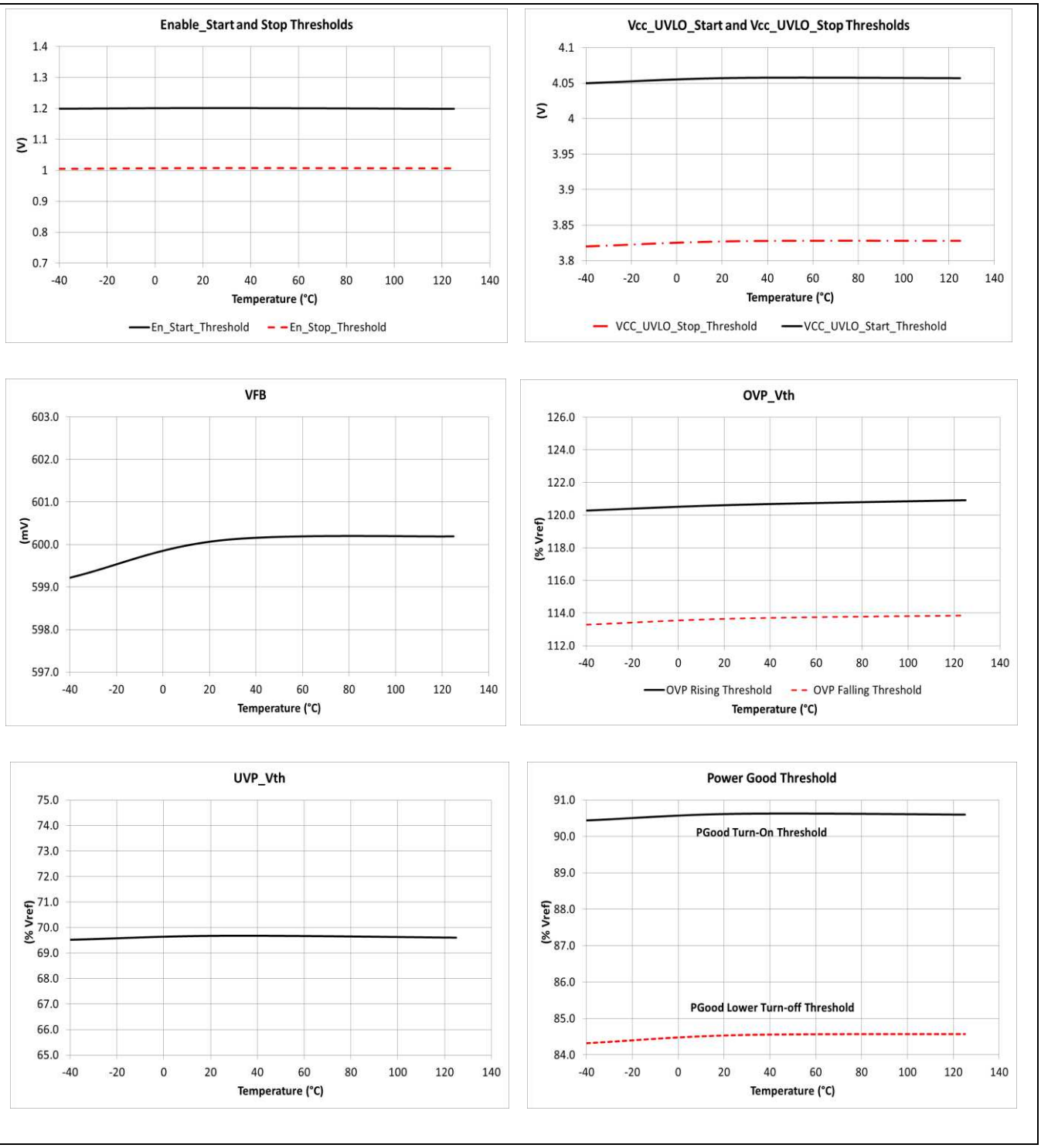


Figure 7 Typical operating characteristics (set 2 of 3)

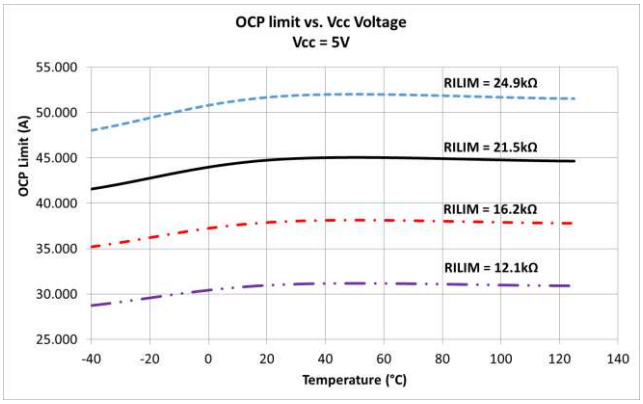


Figure 8 Typical operating characteristics (set 3 of 3)

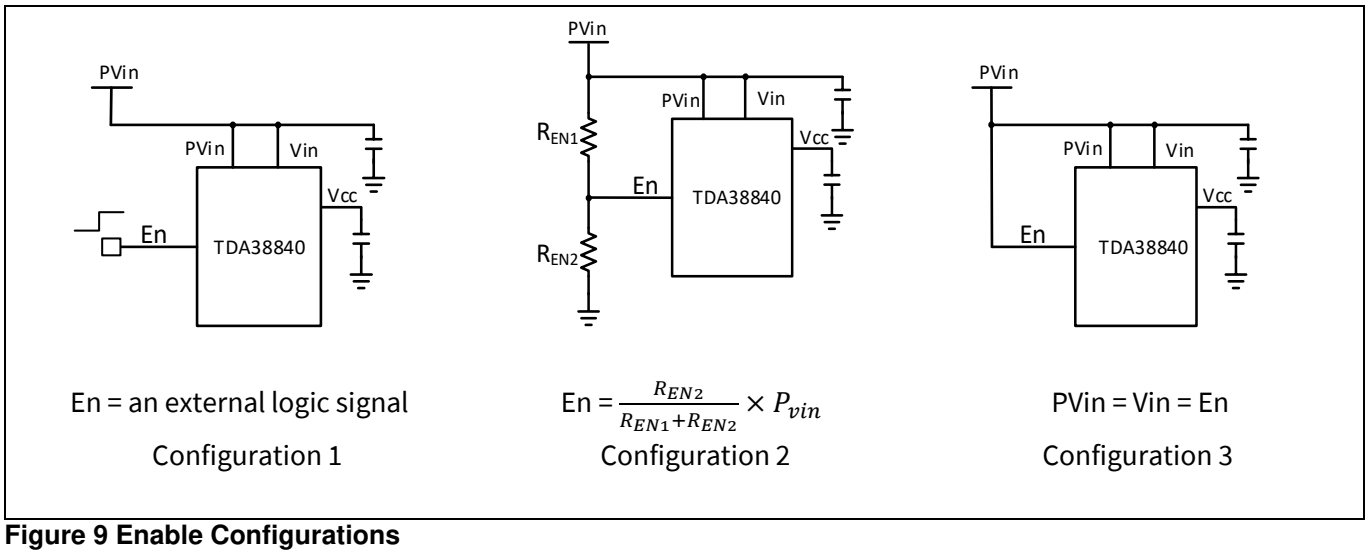
12 Theory of operation

12.1 Fast Constant On-Time Control

The TDA38840 features a proprietary Fast Constant On-Time (COT) Control, which can provide fast load transient response, good output regulation and minimize the design effort. Fast COT control compares the output voltage, Vo, to a floor voltage combined with an internal ramp signal. When Vo drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares the Vo with a reference voltage. Compared to the traditional COT control, Fast COT control significantly improves the Vo regulation.

12.2 Enable

En pin controls the on/off of the TDA38840. An internal Under Voltage Lock-Out (UVLO) circuit monitors the En voltage. When the En voltage is above an internal threshold, the internal LDO starts to ramp up. When the VCC/LDO voltage rises above the VCC_UVLO_Start threshold, the soft-start sequence starts. The En pin can be configured in three ways, as shown in **Figure 9**. With configuration 2, the Enable signal is derived from the PVin voltage by a set of resistive divider, REN1 and REN2. By selecting different divider ratios, users can program a UVLO threshold voltage for the bus voltage. This is a very desirable feature because it prevents the TDA38840 from operating until PVin is higher than a desired voltage level. For some space constrained designs, the En pin can be directly connected to PVin without using the external resistor dividers, as shown in Configuration 3. The En pin should not be left floating. A pull down resistor in the range of tens of kilohms is recommended. **Figure 10** illustrates the corresponding start-up sequences with three En configurations.



En = an external logic signal

Configuration 1

En = $\frac{R_{EN2}}{R_{EN1}+R_{EN2}} \times P_{vin}$

Configuration 2

PVin = Vin = En

Configuration 3

Figure 9 Enable Configurations

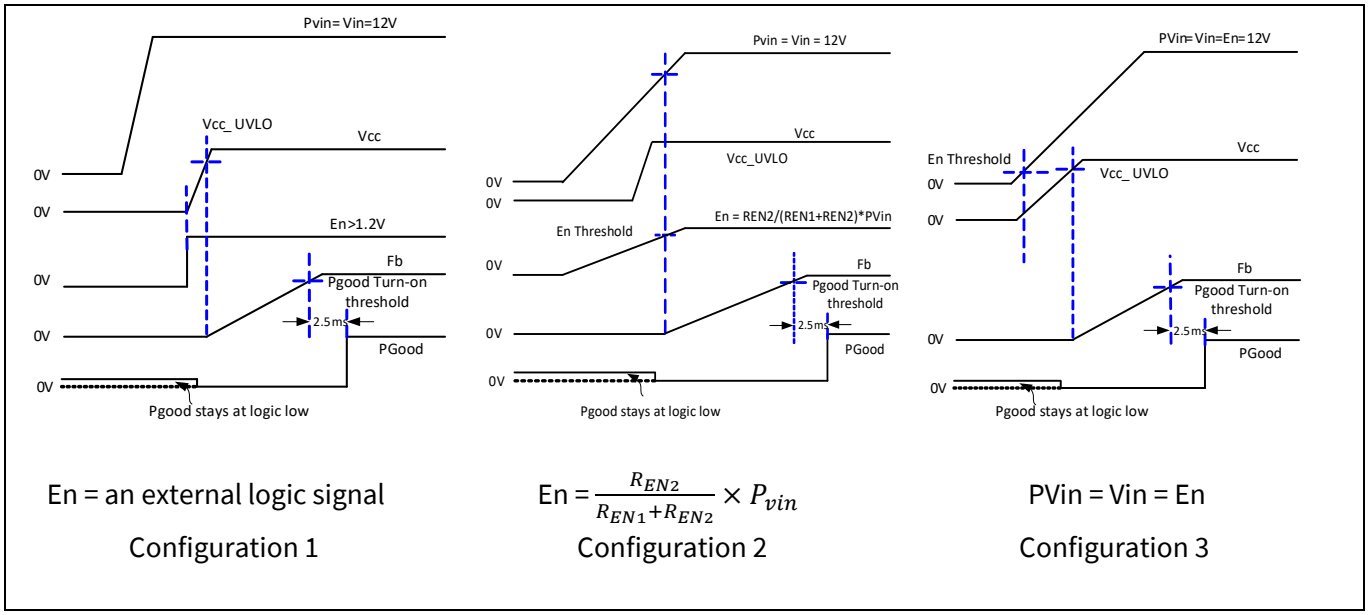


Figure 10 Start-up sequence

12.3 FCCM and DEM Operation

The TDA38840 offers two operation modes: Forced Continuous Conduction (FCCM) and Diode Emulation Mode (DEM). With FCCM, the TDA38840 always operates as a synchronous buck converter with a pseudo constant switching frequency and therefore achieves small output voltage ripples. In DEM, the synchronous FET is turned off when the inductor current is close to zero, which reduces the switching frequency and improves the efficiency at light load. At heavy load, both FCCM and DEM operate in the same way. The operation mode can be selected with TON/MODE pin, as shown in **Table 5**. It should be noted that the selection of the operation mode cannot be changed on the fly. To load a new TON/MODE configuration, En or VCC voltage needs to be cycled.

12.4 Pseudo Constant Switching Frequency

The TDA38840 offers eight programmable switching frequencies, f_{sw}, from 600 kHz to 2 MHz, by connecting an external resistor from TON/MODE pin to a quiet ground (AGND or PGND). Based on the selected f_{sw}, the TDA38840 generates the corresponding on-time of the Control FET for a given PVin and Vo, as shown by the formula below.

$$T_{on} = \frac{V_0}{PV_{in}} \times \frac{1}{f_{sw}}$$

Where fsw is the desired switching frequency. During the operation, the TDA38840 monitors PVin and Vo, and can automatically adjust the on-time to maintain the pre-selected fsw. With the increase of the load, the switching frequency can increase to compensate for the power losses. Therefore, the TDA38840 has a pseudo constant switching frequency.

Table 5 lists the resistors for TON/MODE pin. In this table, E96 resistors with ±1% tolerance are used. If E12 resistor values are preferred, please refer to the Section **12.15**. To load a new TON/MODE configuration, En or VCC voltage needs to be cycled.

Table 5 Configuration Resistors for TON/MODE Pin

TON/MODE Resistor (kΩ) ±1% Tolerance	Freq (kHz)	Mode
0	600	FCCM
1.5	800	
2.49	1000	
3.48	1200	
4.53	1400	
5.76	1600	
7.32	1800	
8.87	2000	
10.5	600	DEM
12.1	800	
14	1000	
16.2	1200	
18.7	1400	
21.5	1600	
24.9	1800	
28.7	2000	
Ton = Floating	800	FCCM

12.5 Soft-start

The TDA38840 has an internal digital soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure a correct start-up, the soft-start sequence initiates when the En and VCC voltages rise above their respective thresholds. The internal soft-start signal linearly rises from 0 V to 0.6 V in a defined time duration. The soft-start time does not change with the output voltage. During the soft-start, the TDA38840 operates in DEM until 1ms after the output voltage ramps above the PGood turn-on threshold. The TDA38840 has four soft-start time options selected by placing a resistor from SS/Latch pin to the ground. **Table 6** lists the resistor values and its corresponding soft-start time. In this table, E96 resistors with ±1% tolerance are used. If E12 resistor values are preferred, please refer to the Section **12.15**. For each soft-start time, there are two resistor options available. Please note that SS/Latch pin is a multi-function pin, which is also used to select different responses for Over Voltage Protection (OVP). Please note that to load a new SS/Latch selection, En or VCC voltage needs to be cycled.

Table 6 Configuration Resistor for SS/Latch Pin

SS/Latch Resistor (kΩ) ±1% Tolerance	Soft-start Time (ms)	OVP
0	1	Latch
4.53		
1.5	2	
5.76		
2.49	4	
7.32		
3.48	8	
8.87		
10.5	1	No Latch
18.7		
12.1	2	
21.5		
14	4	
24.9		
16.2	8	
28.7		
SS/Latch = Floating	4	Latch

12.6 Pre-bias Start-up

The TDA38840 is able to start up into a pre-charged output without causing oscillations and disturbances of the output voltage. When TDA38840 starts up with a pre-biased output voltage, both control FET and Synch FET are kept off till the internal soft-start signal exceeds the FB voltage.

12.7 Internal Low - Dropout (LDO) Regulator

The TDA38840 has an integrated low-dropout LDO regulator, providing the bias voltage for the internal circuitry. To minimize the standby current, the internal LDO is disabled when the En voltage is pulled low. Vin pin is the input of the LDO. When using the internal LDO for a single rail operation, Vin pin should be connected to PVin pin. To save the power losses on the LDO, an external bias voltage can be used by connecting Vin pin to the VCC/LDO pin. VDRV provides the bias voltage for the internal driver circuitry and should be shorted to VCC/LDO on the PCB. **Figure 11** illustrates the configuration of VCC/LDO, VDRV and Vin pin.

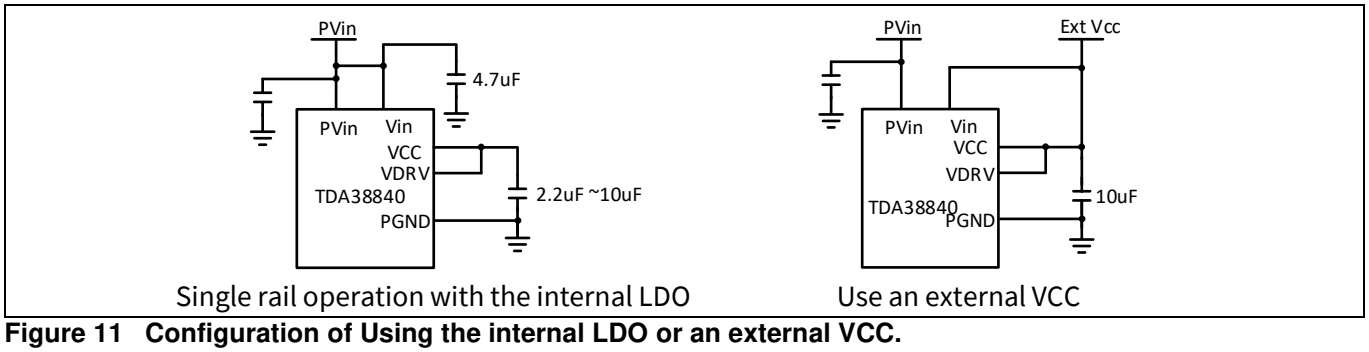


Figure 11 Configuration of Using the internal LDO or an external VCC.

Section 7.1 specified the recommended operating voltage range of Vin and VCC under different configurations. Following design guidelines are recommended when configuring the VCC/LDO.

- Place a bypass capacitor to minimize the disturbance on the VCC and VDRV pin. For a single rail operation using the internal LDO, a 4.7 µF low ESR ceramic capacitor must be used between Vin pin and PGND and a 2.2 µF~10 µF low ESR ceramic capacitor is required to be placed close to the VCC/LDO and VDRV pin with reference to PGND. 10 µF MLCC is recommended for VCC bypass capacitor when Vin is below 5.5 V. When using an external VCC bias voltage, a 10 µF ceramic capacitor can be shared with Vin, VCC/LDO and VDRV pin.
- When using the internal LDO with 5.5 V ≤ Vin ≤ 17 V, it is recommended to check the required VCC bias current for the operation above 1.6 MHz, to ensure that it does not exceed the LDO output current capability as shown in Figure 6. With the increase of fsw, the resulting I_{CC} is also increased mainly due to the increase of the gate charge that is proportional to fsw. In Figure 6, the typical I_{CC} at PVin = Vin = 12 V and fsw = 800 kHz has been provided, which can be used to estimate the I_{CC} at other fsw.
- For applications using the internal LDO with 4.3 V ≤ Vin ≤ 5.4 V, the LDO can be in the dropout mode. It is important to ensure that the LDO voltage does not fall below the VCC UVLO threshold voltage. At Vin = 4.3 V, I_{CC} must not exceed 50 mA under all operating conditions such as during a step-up load transient, in which the control loop may require the increase of fsw. OCP limits can be reduced due to the lower VCC voltage.

12.8 Over Current Protection (OCP)

The TDA38840 offers cycle-by-cycle OCP response with four selectable current limits, which is set by the resistance at ILIM pin. The selected OCP limit bank is loaded to the IC during the power up and cannot be changed on the fly. To change the OCP limit, users must cycle En signal or VCC voltage. Cycle-by-cycle OCP response allows the TDA38840 to fulfill a brief high current demand, such as a high inrush current during the start-up. The detailed operation is explained as follows.

The OCP is activated when En voltage is above its threshold. The OCP circuitry monitors the current of the Synchronous MOSFET through its $R_{ds(on)}$. When a new PWM pulse is requested by the control loop, if the current of Synchronous MOSFET exceeds the selected OCP limit, the TDA38840 skips the PWM pulse and extends the on-time of Synchronous MOSFET till the current drops below the OCP limit. The OCP operation is also illustrated in Figure 12. It should be noted that OCP events do not pull the PGood signal low unless the Vo drops below the PGood turn-off threshold. If the OCP event persists, the output voltage can eventually drop below the Under Voltage Protection (UVP) threshold and trigger UVP. Then the TDA38840 enters a hiccup mode.

The OCP limits specified in the Section 7.2 refer to the valley of the inductor current when OCP is tripped. Therefore, the corresponding output DC current can be calculated as follows:

$$I_{out\_OCP} = I_{OC} + \frac{\Delta i_L}{2}$$

Where: I_{out_OCP} = Output DC current when OCP is tripped. I_{OC} = OCP limit specified in the Section 7.2, which is the valley of inductor current. Δi_L = Peak-peak inductor ripple current. To achieve the desired I_{out_OCP}, Δi_L is recommended to meet the following criterion

$$\Delta i_L \approx 2 \times (I_{out\_OCP} - I_{OC\_min})$$

Where I_{OC_min} = the minimum spec of OCP limit.

To avoid the inductor saturation during OCP events, the following criterion is recommended for the inductor saturation current rating.

$$I_{sat} \geq I_{OC\_max} + \Delta i_L$$

Where: I_{sat} is the inductor saturation current and I_{OC_max} is the maximum spec of the OCP limit.

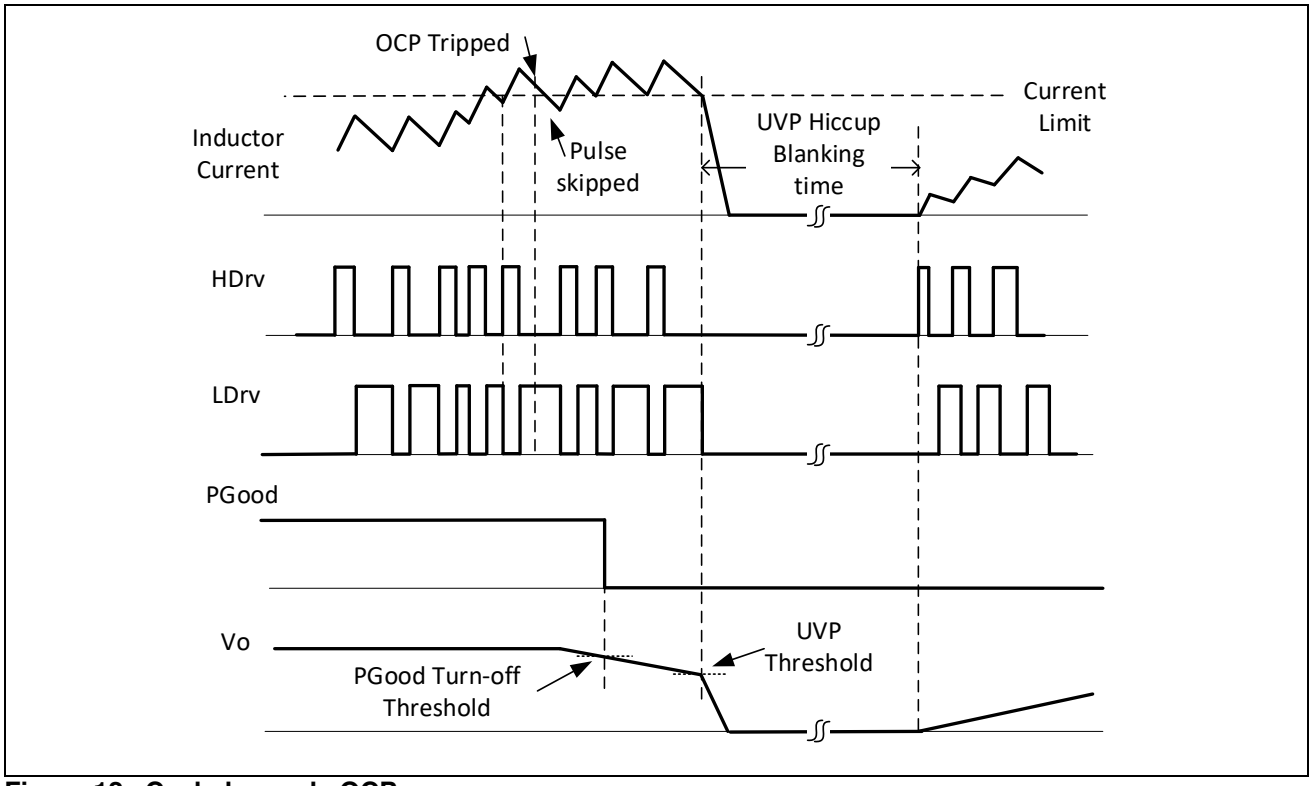


Figure 12 Cycle-by-cycle OCP response

12.9 Under Voltage Protection (UVP)

Under Voltage Protection (UVP) provides additional protection during OCP fault or other faults. UVP is activated when the soft-start voltage rises above 100 mV. UVP circuitry monitors the FB voltage. When it is below the UVP threshold for 2 µs (typical), an under voltage trip signal asserts and both Control MOSFET and Synchronous MOSFET are turned off. The TDA38840 enters a hiccup mode with a blanking time of 20 ms, during which Control MOSFET and Synchronous MOSFET remain off. After the completion of blanking time, the TDA38840 attempts to recover to the nominal output voltage with a soft-start, as shown in **Figure 12**. The TDA38840 will repeat hiccup mode and attempt to recover until UVP condition is removed.

12.10 Over Voltage Protection (OVP)

Over Voltage Protection (OVP) is achieved by comparing the FB voltage to an OVP threshold voltage. When the FB voltage exceeds the OVP threshold, an over voltage trip signal asserts after 8 µs (typical) delay. Control MOSFET is latched off immediately and PGood flags low. Synchronous MOSFET remains on to discharge the output capacitor. When FB voltage drops below around 115% of the reference voltage, Synchronous MOSFET turns off to prevent the complete depletion of the output capacitors. **Figure 13** illustrates the OVP operation. The OVP comparator becomes active when the En signal is above the start threshold.

With SS/Latch pin, two OVP responses can be selected: Latch or No Latch, as shown in **Table 6**. With a latched OVP response, Control FET remains latched off until either VCC voltage or En signal is cycled. With an unlatched OVP response, the TDA38840 enters a hiccup mode. Control FET remains off for a blanking time of 20ms. After hiccup blanking time expires, the TDA38840 will try to restart with a soft-start. The TDA38840 can stay in the hiccup mode infinitely if over voltage fault persists.

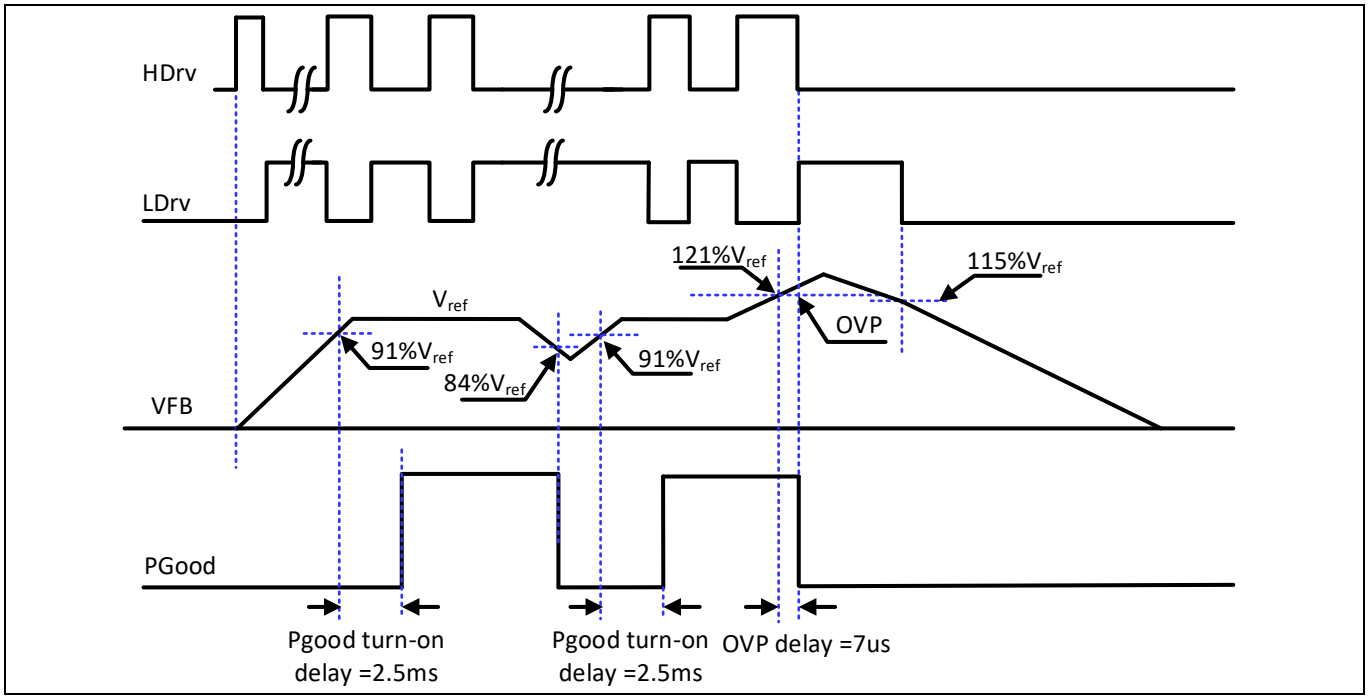


Figure 13 Over voltage protection response and PGood behavior.

12.11 Over Temperature Protection (OTP)

Temperature of the controller is monitored internally. When the temperature exceeds the over temperature threshold, OTP circuitry turns off both Control and Synchronous MOSFETs and resets the internal soft start. Automatic restart is initiated when the sensed temperature drops back into the operating range. The thermal shutdown threshold has a hysteresis of 20 °C.

12.12 Power Good (PGood) Output

The PGood pin is the open drain of an internal NFET, and needs to be externally pulled high through a pull-up resistor. PGood signal is high when three criteria are satisfied.

1. En signal and VCC voltage are above their respective thresholds.

2. No over voltage and over temperature faults occur.

3. V_o is within the regulation.

In order to detect if V_o is in regulation, PGood comparator continuously monitors the FB voltage. When FB voltage ramps up above the upper threshold, PGood signal is pulled high after 2.5 ms. When FB voltage drops below the lower threshold, PGood signal is pulled low immediately. **Figure 13** illustrates the PGood response.

During the start-up with a pre-biased voltage, PGood signal is held low before the first PWM is generated and is then pulled high with 2.5 ms delay after FB voltage rises above the PGood threshold. TDA38840 also integrates an additional PFET in parallel to the PGood NFET, as shown in **Figure 2**. This PFET allows PGood signal to stay at logic low when the VCC voltage is not present, and PGood pin is pulled up by an external bias voltage. Please refer to **Figure 10**. Since PGood PFET has relatively higher on resistance, a 50 kΩ pull-up resistor is needed for a PGood bias voltage of 3.3 V to maintain the PGood signal at logic low when PGood PFET is on.

12.13 Minimum On - Time and Minimum Off - Time

The minimum on-time refers to the shortest time for Control MOSFET to be reliably turned on. The minimum off-time refers to the minimum time duration in which Synchronous FET stays on before a new PWM pulse is generated. The minimum off-time is needed for TDA38840 to charge the bootstrap capacitor, and to sense the current of the Synchronous MOSFET for OCP.

For applications requiring a small duty cycle, it is important that the selected switching frequency results in an on-time larger than the maximum spec of the minimum on-time in the Section **7.2**. Otherwise the resulting switching frequency may be lower than the desired target. Following formula could be used to check for the minimum on-time requirement.

$$\frac{V_0}{f_{sw\_max} \times PV_{in}} > \max\ spec\ of\ T_{on(\min)}$$

For applications requiring a high duty cycle, it is important to make sure a proper switching frequency is selected so that the resulting off-time is longer than the maximum spec of the minimum off-time in the Section **7.2**, which can be calculated as shown below.

$$\frac{PV_{in} - V_0}{f_{sw\_max} \times PV_{in}} > \max\ spec\ of\ T_{off(\min)}$$

Where f_{sw_max} is the maximum switching frequency. In a steady state operation, $f_{sw\_max} = k \cdot f_{sw}$. Where f_{sw} is the desired switching frequency. *k* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to ensure the design margin.

Please note that during a load step, f_{sw} will increase due to the intrinsic COT operation. Therefore it is important to check the change of f_{sw} during the load step. Please also note that OCP limit may be degraded when off-time is close to the minimum off-time.

The resulting maximum duty cycle is therefore determined by the selected on-time and minimum off-time.

$$D_{max} = \frac{T_{on}}{T_{on} + T_{off(\min)}}$$

12.14 Selection of Feedforward Capacitor and Feedback Resistors

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.6 V. The divider ratio is set to provide 0.6 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_o = V_{ref} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

Where R_{FB1} and R_{FB2} are the top and bottom feedback resistors.

A small MLCC capacitor, Cff, is preferred in parallel with the top feedback resistor, RFB1, to provide extra phase boost and to improve the transient load response, as shown in **Figure 14**. Following formula can be used to help select Cff and RFB1. The value of Cff is recommended to be 100 pF or higher to minimize the impact of circuit parasitic capacitance, where Lo and Co are the output LC filter of the buck regulator. **Table 7** lists the suggested m for some common outputs. Cff and RFB1 may be further optimized based on the transient load tests and bode plot measurement. Where Lo and Co are the output LC filter of the buck regulator.

$$R_{FB1}C_{ff} = \frac{\sqrt{L_0 C_0}}{m \times 4.9}$$

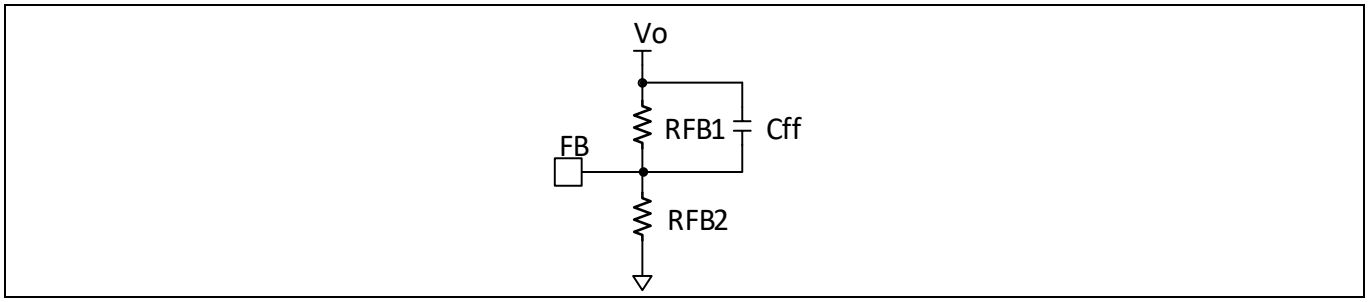


Figure 14 Configuration of feedforward capacitor, Cff.

Table 7 Selection of m

Vo	m
3 V ≤ Vo ≤ 6 V	0.3
1.2 V < Vo < 3 V	0.5
Vo ≤ 1.2 V	0.7

12.15 Resistors for Configuration Pins

To properly configure SS/LATCH pin, MODE/TON pin and ILIM pin, E96 resistors with ±1% tolerance must be used per Table 5, Table 6 and Section 7.2. If E12 resistor values are preferred, the E96 resistors can be replaced with two or three E12 resistors in series, as shown in Table 8. Note that the tolerance of E12 resistors must be ±0.1%.

Table 8 Replacement of E96 configuration resistors with E12 resistors in series

E96 ±1%	E12 ±0.1% (R = R_{S1} + R_{S2} or R_{S1} + R_{S2} + R_{S3})		
R (kΩ)	R_{S1} (kΩ)	R_{S2} (kΩ)	R_{S3} (kΩ)
4.53	2.7	1.8	N/A
1.50	1.5	0	N/A
5.76	5.6	0.15	N/A
2.49	1.8	0.68	N/A
7.32	6.8	0.56	N/A
3.45	3.3	0.15	N/A
8.87	8.2	0.68	N/A
10.5	10	0.47	N/A
12.1	12	0.1	N/A
21.5	18	3.3	N/A
14	10	3.9	N/A
24.9	22	2.7	N/A
16.2	15	1.2	N/A
28.7	27	1.8	N/A
21.5	18	3.3	0.18
24.9	22	2.7	0.18

13 Design example

In this section, an example is used to explain how to design a buck regulator with the TDA38840. The application circuit is shown in Figure 15. The design specifications are given below.

- PVin = 12 V (±10%)
- Vo = 1.0 V
- Io = 40 A
- Vo ripple voltage = ±1% of Vo
- Load transient response = ± 4% of Vo with a step load current = 12 A and slew rate = 10 A/µs

13.1 Enabling the TDA38840

The TDA38840 has a precise En threshold voltage, which can be used to implement a UVLO of the input bus voltage by connecting the En pin to PVin with a resistor divider, as shown in Configuration 2 of Figure 9. The En resistor divider, R_{EN1} and R_{EN2}, can be calculated as follows.

$$PV_{in(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq V_{EN(\max)}$$

$$R_{EN2} \geq R_{EN1} \times \frac{V_{EN(\max)}}{PV_{in(\min)} - V_{EN(\max)}}$$

Where $V_{EN(max)}$ is the maximum spec of the En-start-threshold as defined in Section **7.2**. For PVin $_{(min)}$=10.8 V, select R_{EN1}=49.9 kΩ and R_{EN2}=7.5 kΩ.

13.2 Programming the Switching Frequency and Operation Mode

The TDA38840 has very good efficiency performance and is suitable for high switching frequency operation. In this case, 800 kHz is selected to achieve a good compromise between the efficiency, passive component size and dynamic response. In addition, FCCM operation is selected to ensure a small output ripple voltage over the entire load range. To select 800 kHz and FCCM operation, the TON/MODE pin can be left floating or connect a 1.5 kΩ resistor to a quiet ground (AGND or PGND) per **Table 5**.

13.3 Selecting Input Capacitors

Without input capacitors, the pulse current of Control MOSFET is directly from the input supply power. Due to the impedance on the cable, the pulse current can cause disturbance on the input voltage and potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_o}{PV_{in}}$$

Where I_{RMS} is the RMS value of the input capacitor current. I_o is the output current and D is the Duty Cycle. For I_o = 40A and $D_{(max)}$ = 0.09, the resulting RMS current flowing into the input capacitor is I_{rms} = 11.6 A.

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

$$C_{in(\min)} > \frac{I_o \times (1-D) \times D}{f_{sw} \times (\Delta PV_{in} - ESR \times I_o \times (1-D))}$$

Where ΔPVin is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistor of the input capacitors. Ceramic capacitors are recommended due to low ESR, ESL and high RMS current capability. For Io = 40 A, fsw = 800 kHz, ESR = 3 mΩ, and ΔPVin = 240 mV, $Cin_{(min)}$ > 32 µF. To account for the de-rating of ceramic capacitors under a bias voltage, 10 x 22 µF/0805/25V MLCC are used for the input capacitors. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

13.4 Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20% and 60% of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core material, inductor saturation current may decrease as the increase of temperature. So it is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relation:

$$L = (PV_{in(\max)} - V_o) \times \frac{D_{min}}{\Delta i_{L(\max)} \times F_{sw}}$$

$$D_{min} = \frac{V_o}{PV_{in(\max)}}$$

$$I_{sat} \geq OCP_{max} + \Delta i_{L(\max)}$$

Where: $PVin_{(max)}$ = Maximum input voltage; ΔiL_{max} = Maximum peak-to-peak inductor ripple current; OCP_{max} = maximum spec of the OCP limit as defined in Section **7.2**; and I_{sat} = inductor saturation current. In this case, select inductor L =120 nH to achieve ΔiL_{max} = 27% of I_{omax}. The I_{sat} should be no less than 66 A.

13.5 Output Capacitor Selection

The output capacitor selection is mainly determined by the output voltage ripple and transient requirements.

To satisfy the Vo ripple requirement, C_o should satisfy the following criterion.

$$C_o > \frac{\Delta i_{Lmax}}{8 \times \Delta V_{or} \times f_{sw}}$$

Where ΔV_{or} is the desired peak-to-peak output ripple voltage. For ΔiL_{max}= 9.6 A, ΔV_{or} =20 mV, fsw = 800 kHz, C_o must be larger than 75 µF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use Multi-Layer Ceramic Capacitor (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion.

$$C_o > \frac{L \times \Delta I^2_{o(\max)}}{2 \times \Delta V_{oL} \times V_o}$$

Where ΔV_{OL} is the allowable Vo deviation during the load transient. $\Delta Io_{(max)}$ is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet the transient requirements. As a rule of thumb, we can triple the Co that is calculated above as a starting point, and then optimize the design based on the bench measurement. In this case, to meet the transient load requirement (i.e. ΔV_{OL}= 40 mV, $\Delta Io_{(max)}$ = 12 A), calculated Co = ~648 µF, select 800 µF in the final design. For more accurate estimation of Co, simulation tool should be used to aid the design.

13.6 Output Voltage Programming

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.6 V. The divider ratio is set to provide 0.6 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_o = V_{ref} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

Where R_{FB1} and R_{FB2} are the top and bottom feedback resistors. Select R_{FB1} = 7.5 kΩ and R_{FB2} = 11.3 kΩ, to achieve Vo = 1 V.

13.7 Feedforward Capacitor

A small MLCC capacitor, C_{ff}, can be placed in parallel with the top feedback resistor, R_{FB1}, to improve the transient response. Based on Section **12.14**, C_{ff} can be selected using the following formula.

$$R_{FB1}C_{ff} = \frac{\sqrt{L_0 C_0}}{0.7 \times 4.9}$$

With Lo = 120 nH, Co = 800 µF and R_{FB1} = 7.5 kΩ, C_{ff} = ~ 300 pF. C_{ff} can be further optimized on the bench test based on bode plot measurement and transient load response.

13.8 Bootstrap Capacitor

For most applications, a 0.1 µF ceramic capacitor is recommended for bootstrap capacitor placed between PHASE and BOOT Pin. To ensure the maximum SW node spike voltage does not exceed 20 V, a 2 Ω resistor is used in series with the BOOT pin on the EVAL_38840_1Vout evaluation board. The resistance should be optimized with different PCB layout design and operation conditions.

13.9 Vin, VCC/LDO and VDRV bypass Capacitor

Please see the recommendation in **Section 12.7**. A 10 µF MLCC is selected for VCC/LDO and VDRV bypass capacitor and a 4.7 µF MLCC is selected for Vin bypass capacitor.

14 Application Information

14.1 Application Diagram

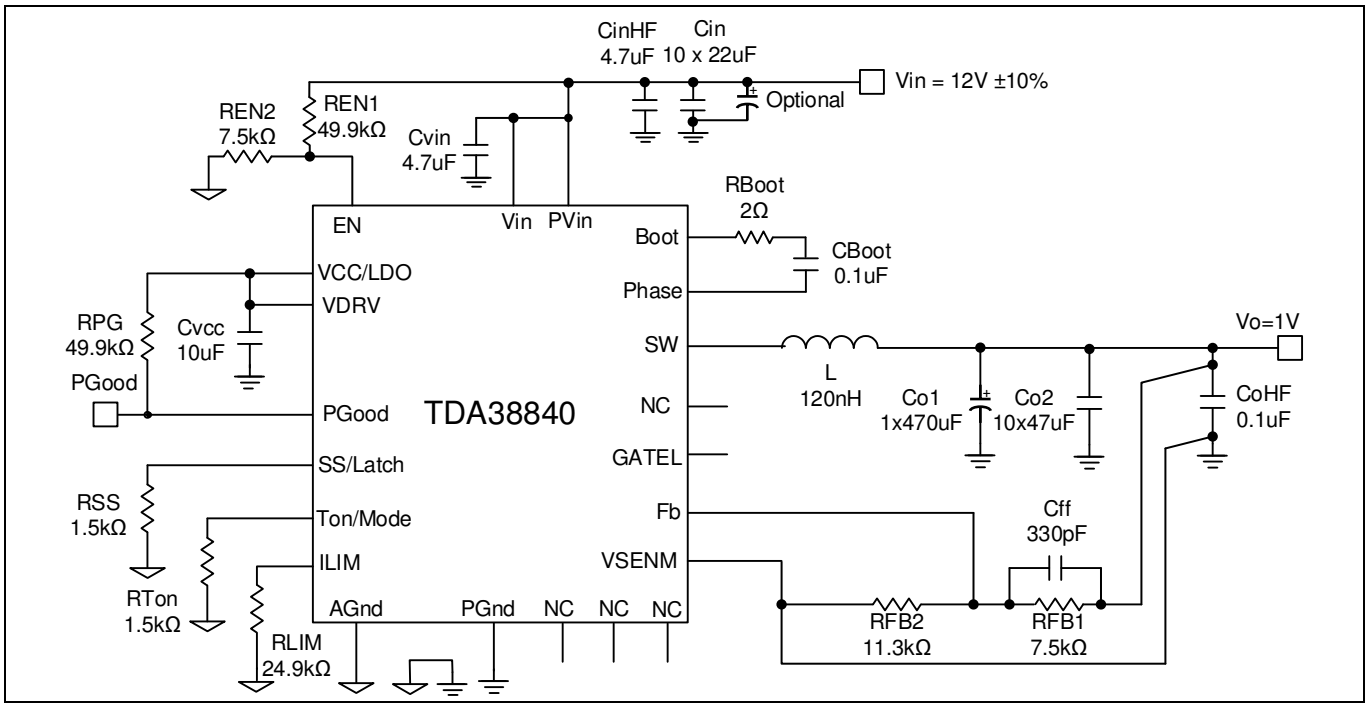


Figure 15 Application diagram of TDA38840. PVin = 12 V, Vo = 1V, Io = 40 A, fsw = 800 kHz.

14.2 Typical Operating Waveforms

PVin = Vin = 12.0 V, Vo = 1 V, Io = 0 – 40 A, fsw = 800 kHz, Room Temperature, no airflow

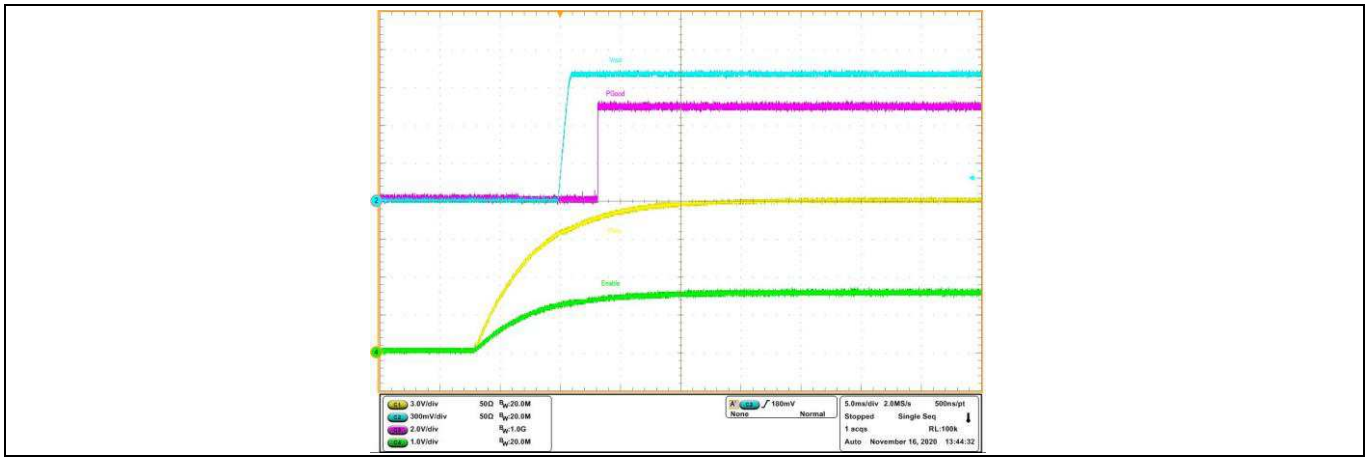


Figure 16 Start up at 40 A Load, (Ch_1: PVin, Ch_4: Enable, Ch_3:PGood ,Ch_4:Vout)

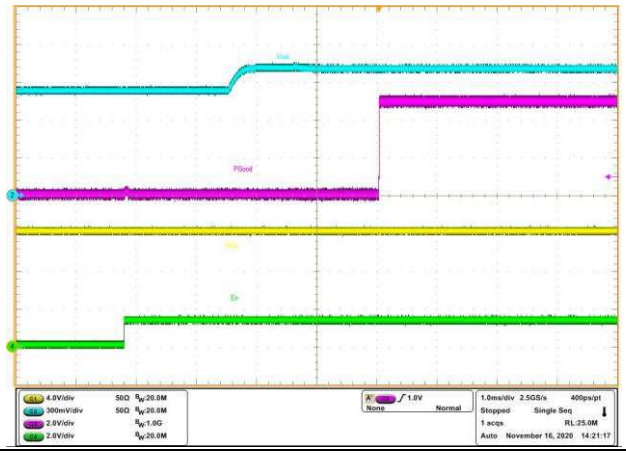


Figure 17 Pre-bias Start up at 0 A Load, (Ch_1: PVin, Ch_2: Vo, Ch_3: PGood, Ch_4: Enable).

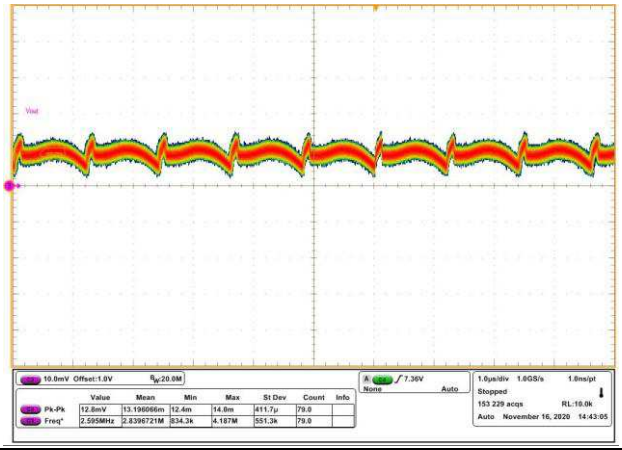


Figure 18 Vo ripple at 40 A Load, fsw = 800 kHz, (Ch_3: Vo), peak to peak Vo ripple = 12.8 mV

Figure 19 SW node, 40 A load, fsw = 800 kHz

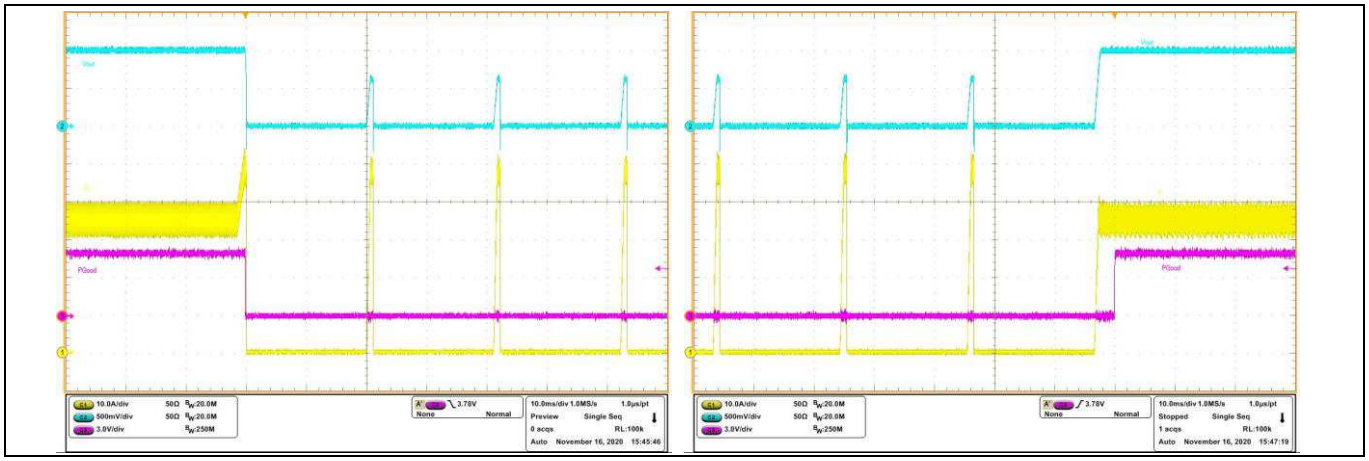


Figure 20 Left: Shorted Vout, and UVP (Hiccup), right: remove short circuit at Vout and TDA38840 recovers from UVP. (Ch1: iL, Ch2: Vo, Ch3:PGood)

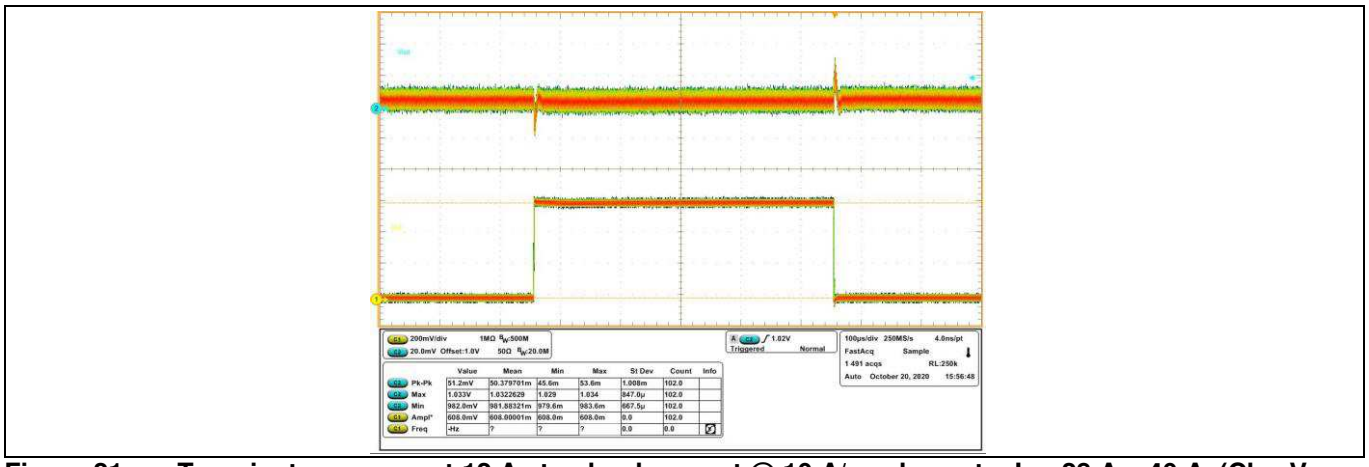


Figure 21 Transient response at 12 A step load current @ 10 A/µs slew rate: Io= 28 A – 40 A, (Ch$_1$: Vo, Ch$_4$: Io exclude 28 A DC current), pk-pk: 51.2 mV, fsw = 800 kHz

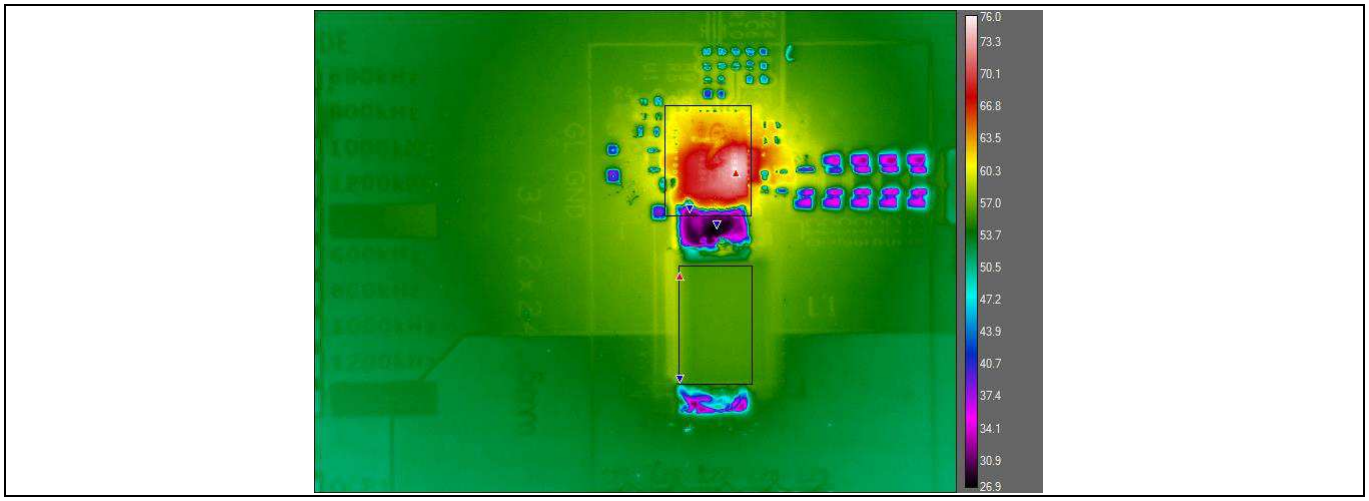


Figure 22 Thermal image of the board at 40 A load TDA38840 = 76°C, L = 57°C, fsw = 800 kHz, Ta = room temperature, natural convection

15 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results. Following design guidelines are recommended to achieve the best performance.

- Bypass capacitors, including input/output capacitors, Vin, VCC and VDRV bypass capacitors, should be placed near the corresponding pins as close as possible.
- Place bypass capacitors from TDA38840 power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate the switching spikes on the Vo. The bypass capacitor shared by VCC and VDRV should be terminated to PGND.
- Place a boot strap capacitor near the TDA38840 BOOT and PHASE pin as close as possible to minimize the loop inductance.
- SW node copper should only be routed on the top layer to minimize the impact of switching noises
- Connect AGND pin to the PGND pad through a single point connection. On the TDA38840 demo board, AGND pin is connected to the exposed PGND pad with a copper trace.
- Via holes can be placed on PVin and PGND pads to aid thermal dissipation.
- Wide copper polygons are desired for PVin and PGND connections in favor of power losses reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers.
- Single-ended Vo sensing is often used for local sensing. To implement this configuration, following design guidelines should be followed, as illustrated in **Figure 23**.
    - The output voltage can be sensed from a high-frequency bypass capacitor of 0.1 µF or higher, through a 15 mil PCB trace.
    - Keep the Vo sense line away from any noise sources and shield the sense line with ground planes.
    - The sense trace is connected to a feedback resistor divider with the lower resistor terminated at VSENM pin.
    - Short VSENM pin and AGND pin with a short trace.
- If it is required to sense the output voltage at a remote location, pseudo remoting sensing can be implemented as follows. The configuration is also shown in **Figure 24**.
    - A pair of PCB traces with at least 15 mil trace width, running close to each other and away from any noise sources such as inductor and SW nodes, should be used to implement Kelvin sensing of the voltage across a high bypass capacitor of 0.1 µF or higher.
    - The ground connection of the remote sensing signal must be terminated at VSENM pin.
    - The Vo connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at VSENM pin.
    - Shield the pair of remote sensing lines with ground planes above and below.
    - Do **NOT** connect VSENM pin and AGND pin in this configuration
- The En pin and configuration pins including SS/LATCH, TON/MODE, and ILIM should be terminated to a quiet ground. On the TDA38840 standard demo board, they are terminated to the PGND copper plane away from the power current flow. Alternatively, they can be terminated to a dedicated AGND PCB trace.

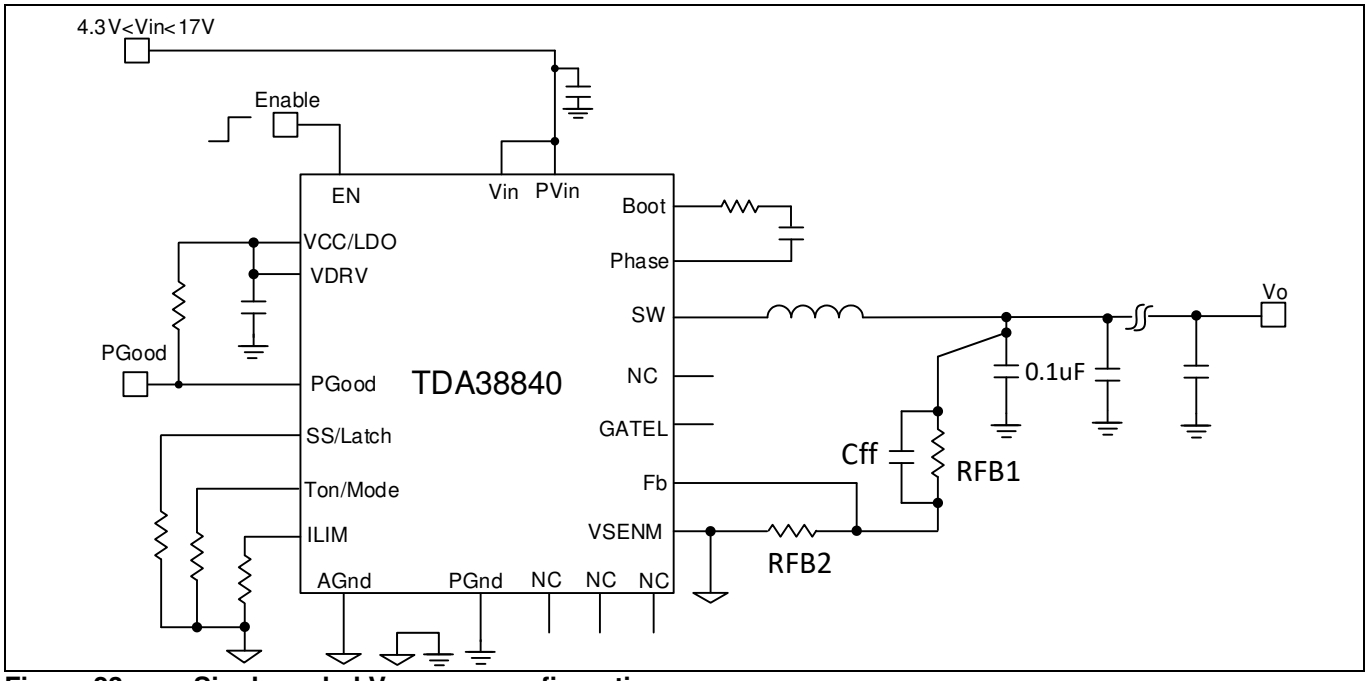


Figure 23 Single-ended Vo sense configuration

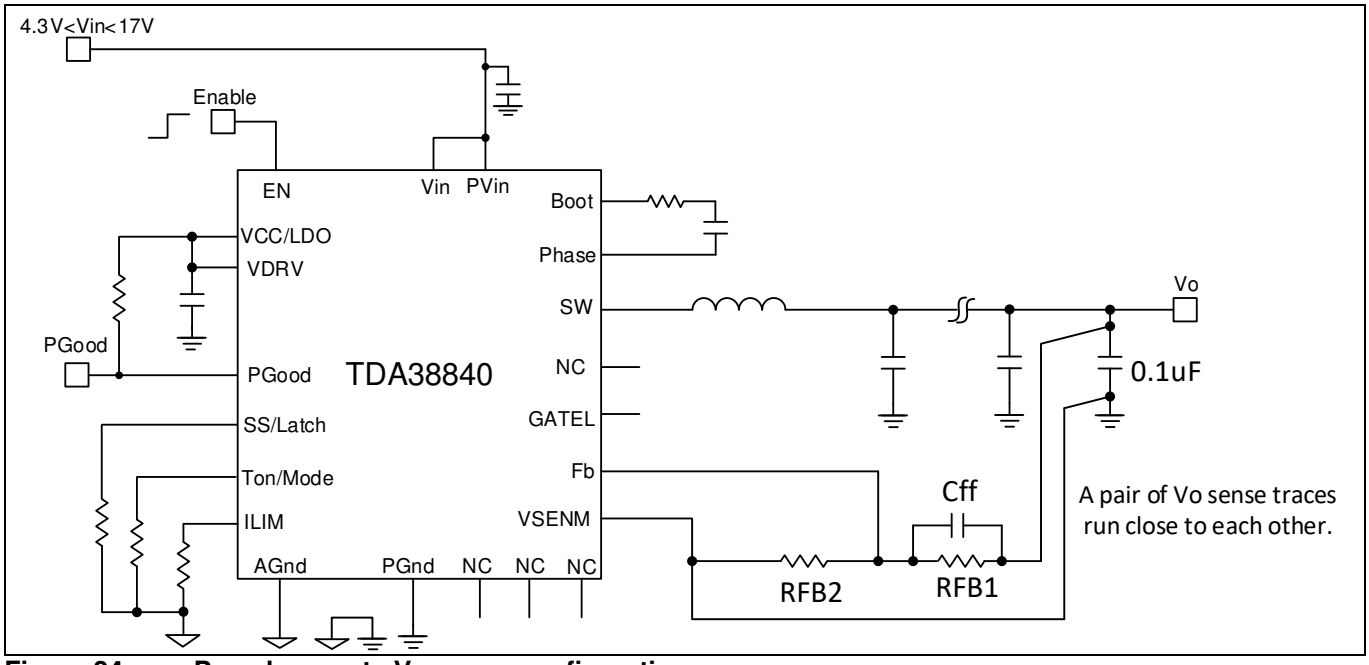


Figure 24 Pseudo remote Vo sense configuration

Following figures illustrate the PCB layout design of the TDA38840 standard demo board with pseudo remote V_o sense.

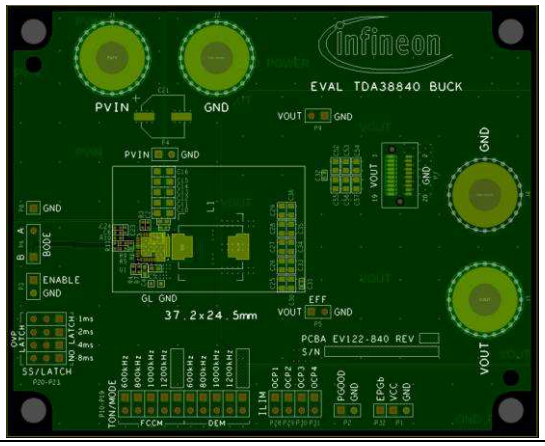


Figure 25 TDA38840 Demo Board – Top Layer

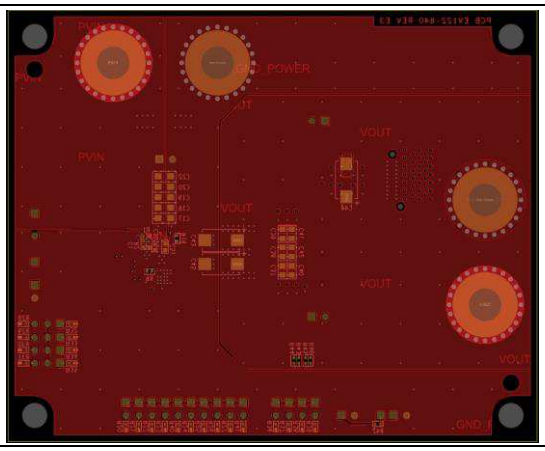


Figure 26 TDA38840 Demo Board – Bottom Layer

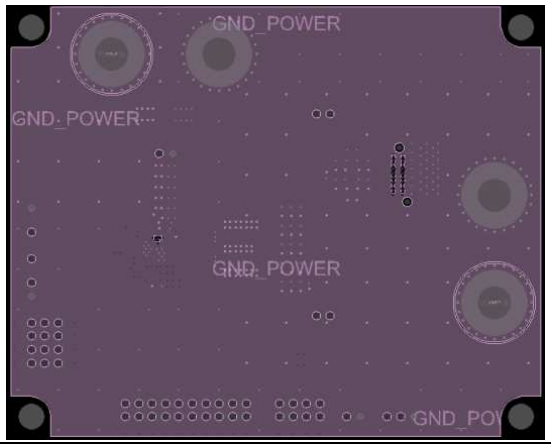


Figure 27 Mid layer 1

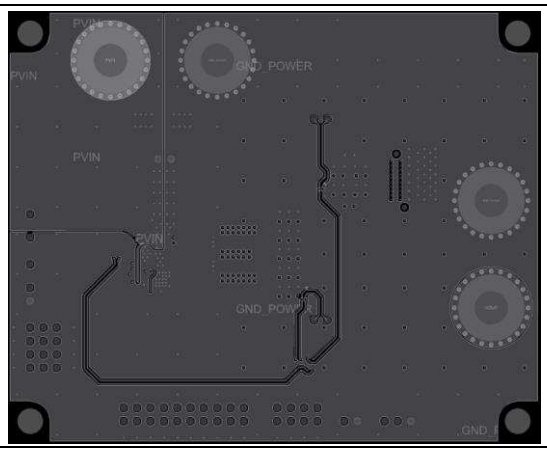


Figure 28 Mid layer 2

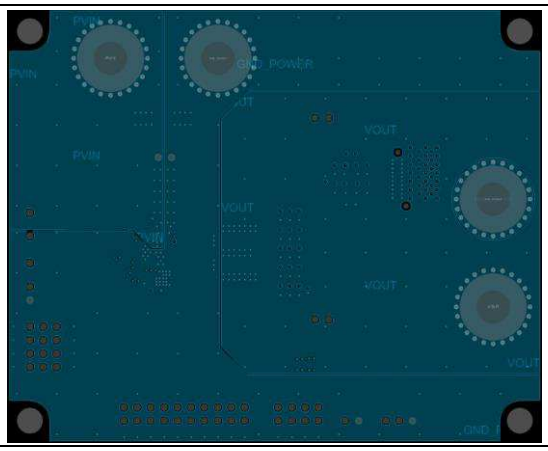


Figure 29 Mid layer 3

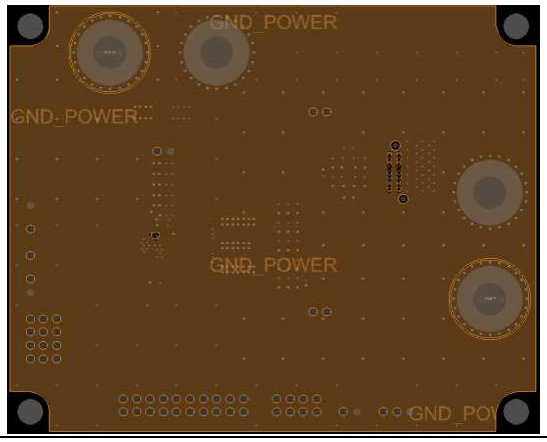


Figure 30 Mid layer 4

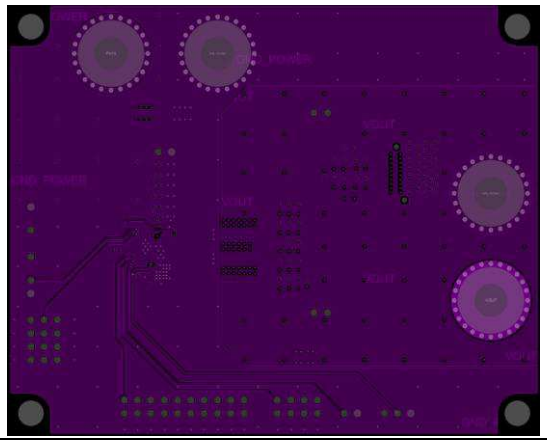


Figure 31 Mid layer 5

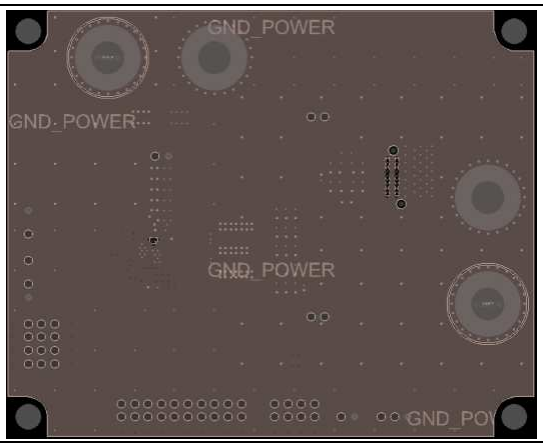


Figure 32 Mid layer 6

15.1 Solder Mask

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD). This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes. Ensure that the solder resist in-between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

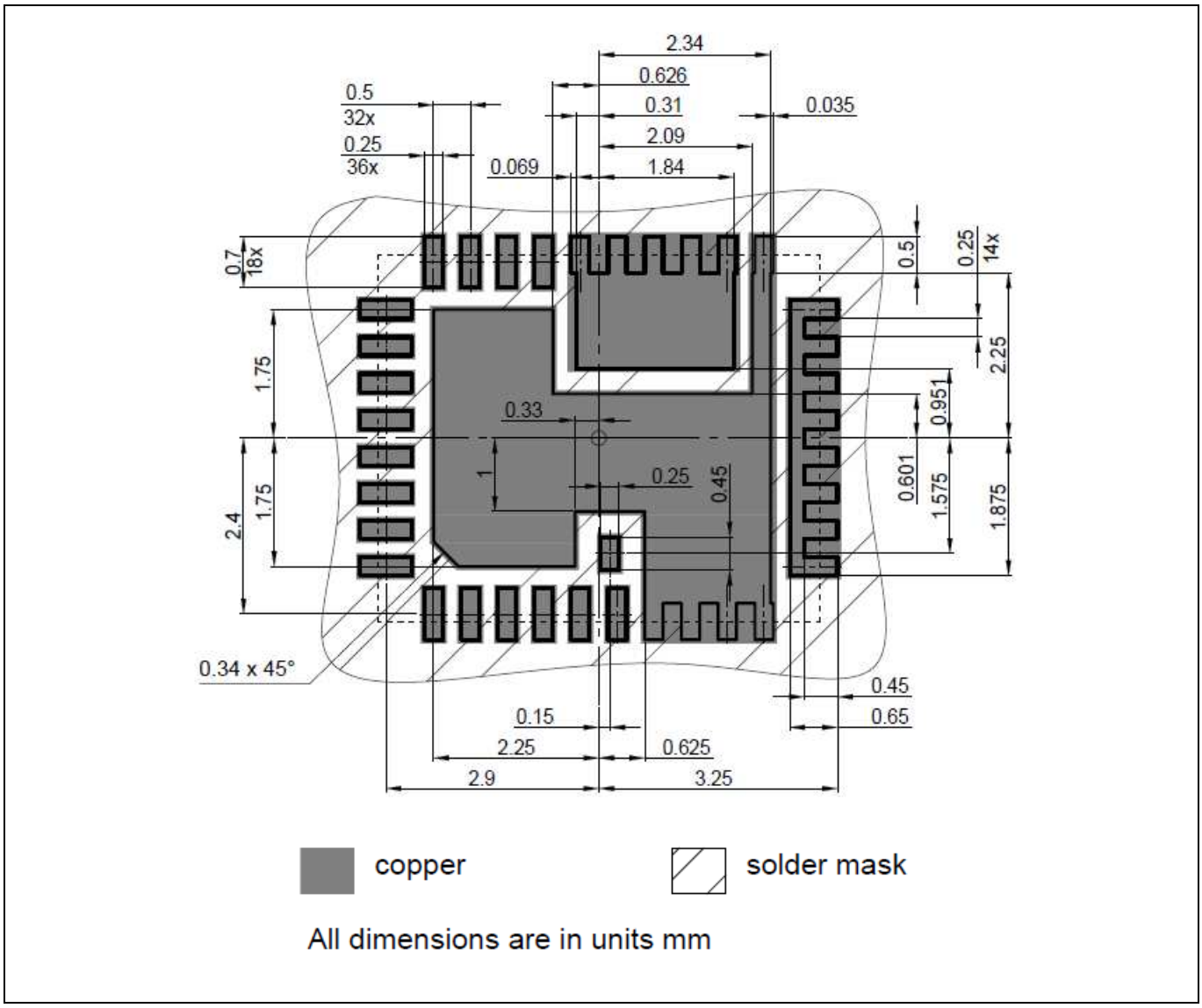


Figure 33 Solder mask (all dimensions in mm)

15.2 Stencil Design

In most cases, the thickness of a stencil has to be matched to the needs of all components on the PCB. For typical integrated QFN or SON packages, stencils with a thickness of 100 µm to 120 µm are recommended. Further details and specific stencil design recommendations can be found in the application note "Recommendations for Board Assembly of Infineon Integrated Packages without Leads". A recommended stencil design is shown below. This design is for a stencil thickness of 100 µm.

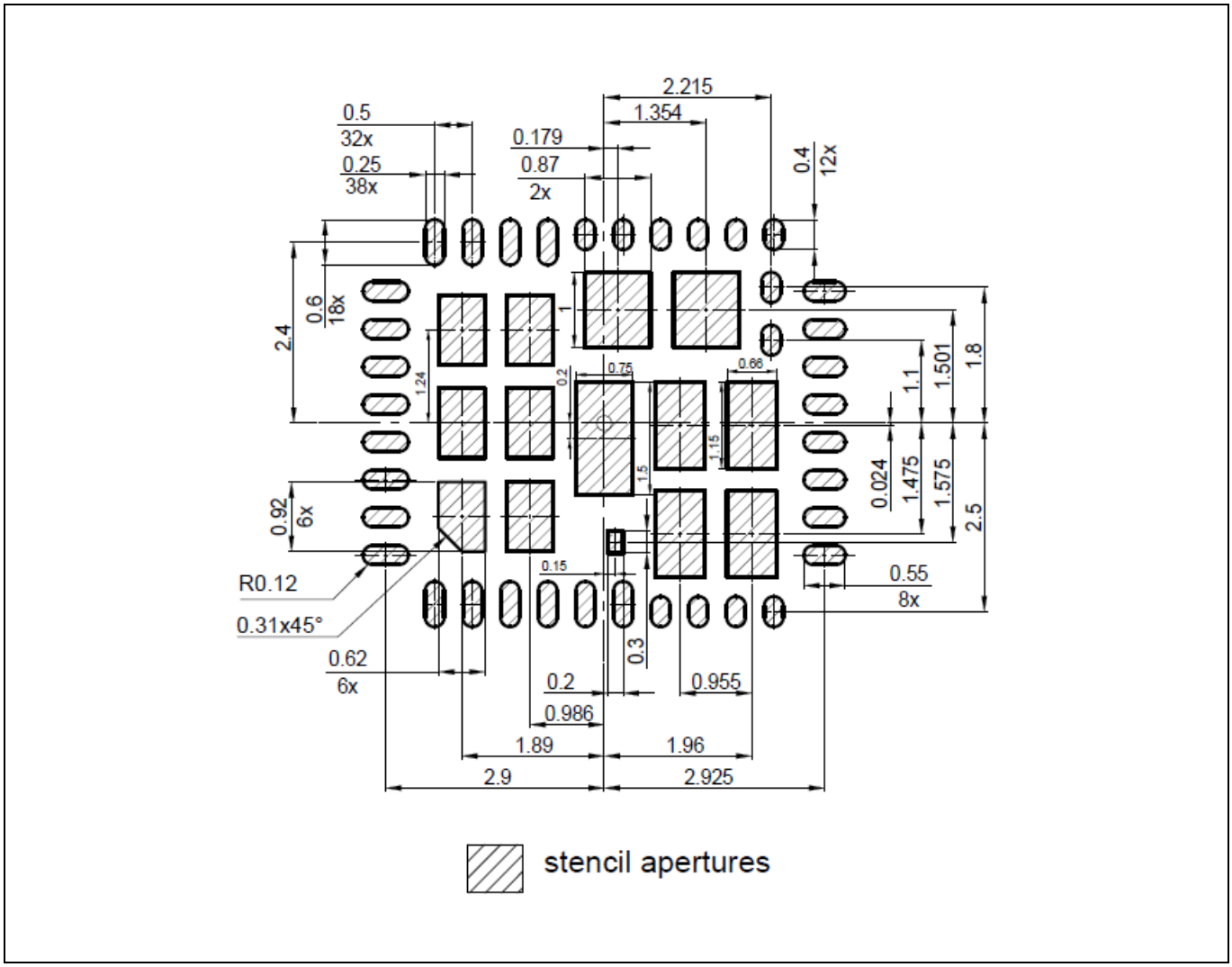


Figure 34 Stencil pad size and spacing (all dimensions in mm)

16 Package

This section includes marking, mechanical and packaging information for the TDA38840.

16.1 Marking Information

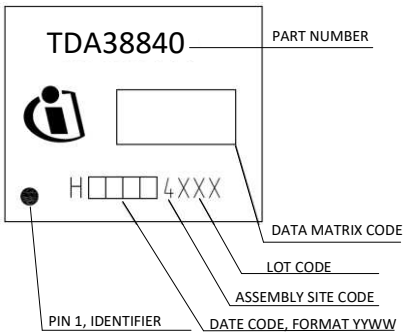
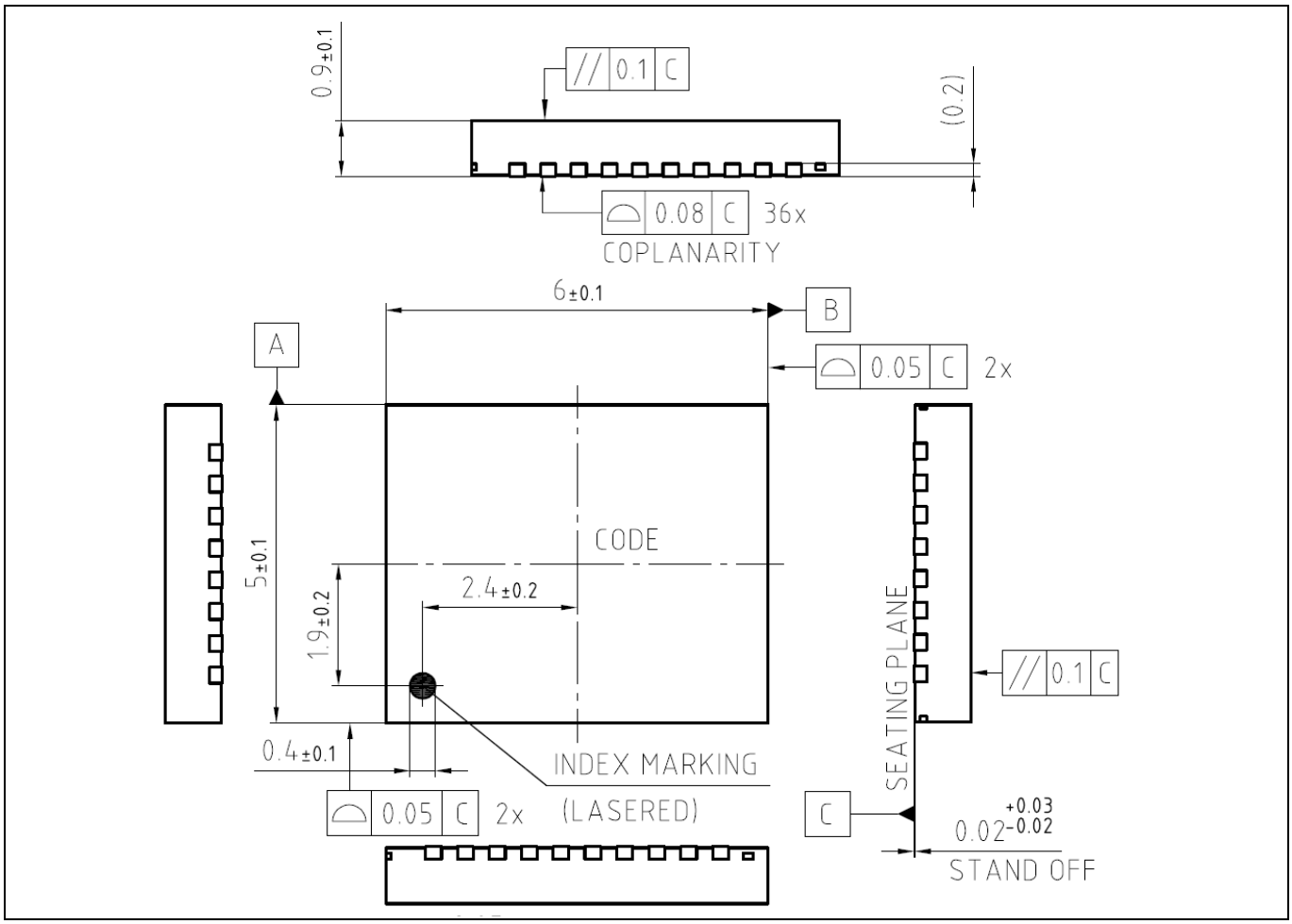


Figure 35 Package Marking

16.2 Dimensions



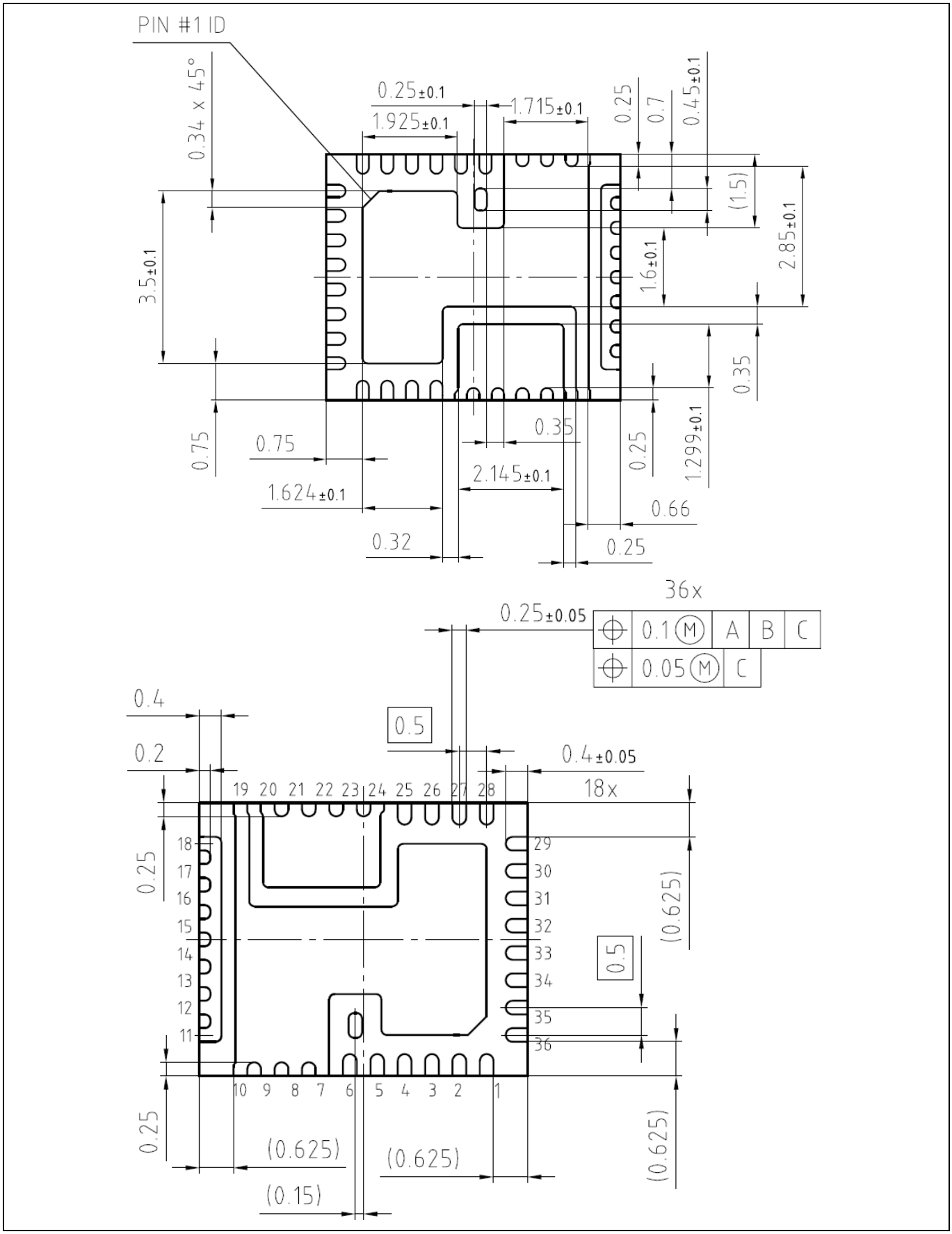


Figure 36 Package Dimensions (all dimensions in mm)

16.3 Tape and Reel Information

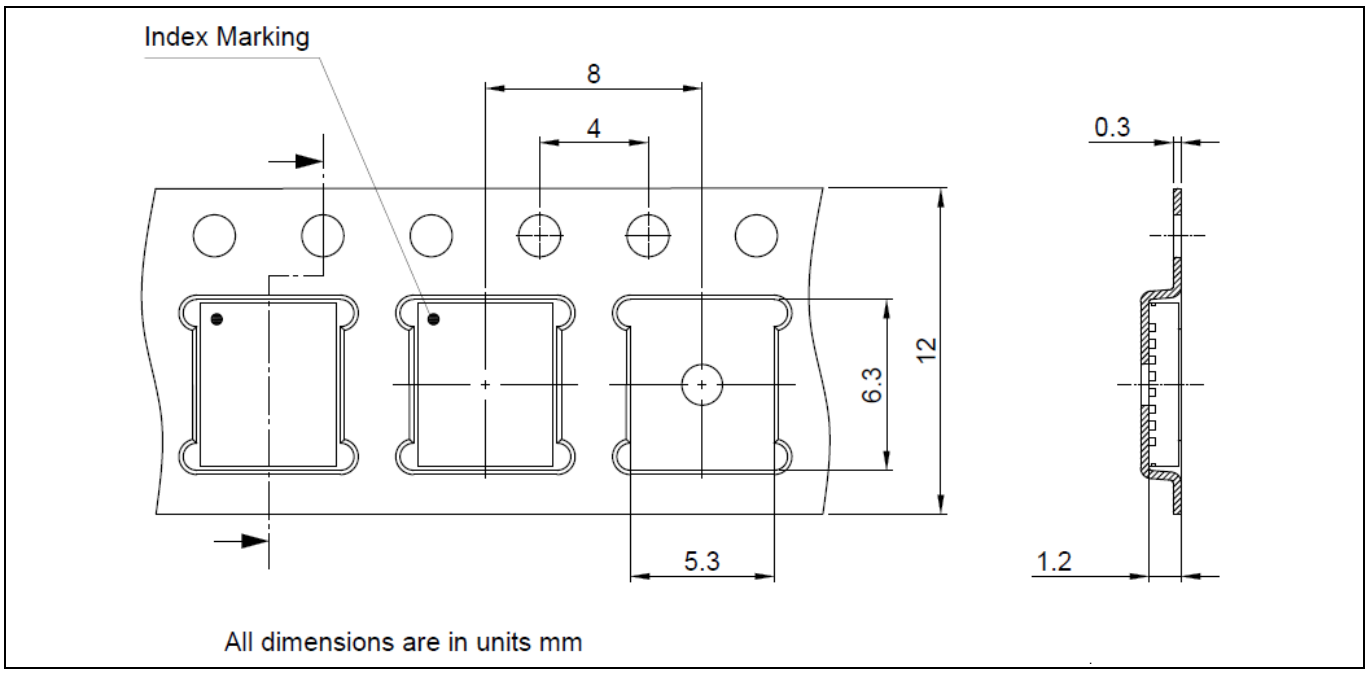


Figure 37 Pin 1 orientation in the tape

17 Environmental Qualifications

Qualification Level		**Industrial**	
Moisture Sensitivity		QFN Package	JEDEC Level 2 @ 260 °C
ESD	Human Body Model	ANSI/ESDA/JEDEC JS-001, 2 (2000 V to < 4000 V)	
	Charged Device Model	ANSI/ESDA/JEDEC JS-002, C3 (≥1000 V)	
RoHS2 Compliant		This product is in compliance with EU Directive 2015/863/EU amending Annex II to EU Directive 2011/65/EU (RoHS) and contains Pb according RoHS exemption 7a, Lead in high melting temperature type solders.	

18 Evaluation Boards and Support Documentation

Table 9 TDA38840 Evaluation Boards and User Guides

Evaluation board	Specifications	Website Address
EVAL_38840_1Vout	12 V±10%, 1 V, 40 A	www.infineon.com/ EVAL_38840_1Vout

Table 10 TDA38840 Package Information

Device	Package Type	Website Address
TDA38840	PG-IQFN-36-2	https://www.infineon.com/cms/en/product/packages/PG-IQFN

Revision History

TDA38840

Revision: 2022-04-13, Rev. 2.2

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2021-04-17	Release of final version
2.1	2021-06-15	Update Table 7
2.2	2022-04-13	Update figure 33, 34, and 37

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