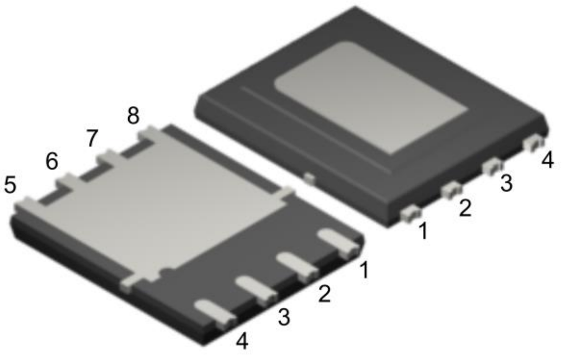
# STLD125N4F6AG

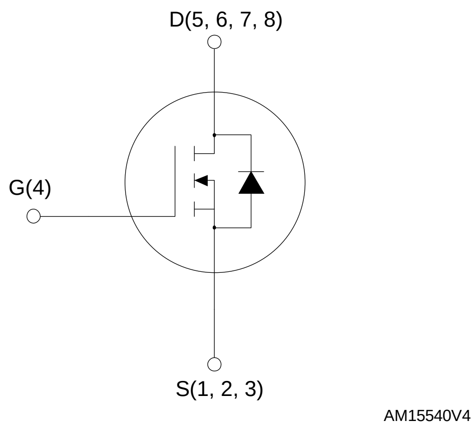
## Automotive N-channel 40 V, 2.4 mΩ typ., 120 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 dual side cooling

Datasheet - preliminary data




PowerFLAT™ 5x6 double side cooling

Figure 1: Internal schematic diagram




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STLD125N4F6AG | 40 V | 3.0 mΩ | 120 A |

- Designed for automotive applications
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STLD125N4F6AG | 125 | PowerFLAT™ 5x6 dual side cooling | Tape and reel |



This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

# Contents

# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 40 | V |
| $V_{GS}$ | Gate-source voltage | ± 20 | V |
| $I_D$ (1)(2) | Drain current (continuous) at $T_C$ = 25 °C | 120 | A |
| $I_D$ (2) | Drain current (continuous) at $T_C$ = 100 °C | 101 | A |
| $I_{DM}$ (2)(3) | Drain current (pulsed) | 480 | A |
| $P_{TOT}$ (2) | Total dissipation at $T_C$ = 25 °C | 130 | W |
| $T_J$ | Operating junction temperature range | - 55 to 175 | °C |
| $T_{stg}$ | Storage temperature range | | |

**Notes:**

(1)Limited by package.

(2)The value is rated according to $R_{thj\text{-}case\ bottom\ side}$.

(3)Pulse width limited by safe operating area.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}c\ top\ side}$ | Thermal resistance junction-case top side | 2.9 | °C/W |
| $R_{thj\text{-}c\ bottom\ side}$ | Thermal resistance junction-case bottom side | 1.14 | |
| $R_{thj\text{-}pcb}$ (1) | Thermal resistance junction-pcb | 31.3 | |

**Notes:**

(1)When mounted on 1 inch² 2 Oz. Cu board, t ≤ 10 s

Table 4: Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AV}$ | Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature) | 90 | A |
| $E_{AS}$ | Single pulse avalanche energy ($T_j$ = 25 °C, $I_C$ = $I_{AV}$, $V_{DD}$ = 16 V) | 150 | mJ |

# 2 Electrical characteristics

($T_C$= 25 °C unless otherwise specified)

**Table 5: On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 40 | | | V |
| $I_{DSS}$ | Zero gate voltage Drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 16 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 16 V, Tj = 125 °C(1) | | | 10 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 1 mA | 2 | | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 75 A | | 2.4 | 3 | mΩ |
| | | $V_{GS}$ = 6.5 V, $I_D$ = 75 A | | 2.7 | 3.5 | |

**Notes:**

(1)Defined by design. Not subject to production test.

**Table 6: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$= 10 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 5600 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 890 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 560 | - | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 32 V, $I_D$ = 75 A, $V_{GS}$ = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*) | - | 91 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 28 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 27 | - | nC |

**Table 7: Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 30 V, $I_D$ = 75 A $R_G$ = 30 Ω, $V_{GS}$ = 10 V (see *Figure 13: "Test circuit for resistive load switching times"*) | - | 47 | - | ns |
| $t_r$ | Rise time | | - | 300 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 255 | - | ns |
| $t_f$ | Fall time | | - | 220 | - | ns |

**Table 8: Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$[(1)] | Source-drain current | | - | | 120 | A |
| $I_{SDM}$[(1)(2)] | Source-drain current (pulsed) | | - | | 480 | A |
| $V_{SD}$ [(3)] | Forward on voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 90 A | - | | 1.2 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 90 A, di/dt = 100 A/µs, $V_{DD}$ = 20 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*) | - | 40 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 41 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 2 | | A |

**Notes:**

(1)Limited by package.

(2)Pulse width is limited by safe operating area

(3)Pulse test: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2: Safe operating area**

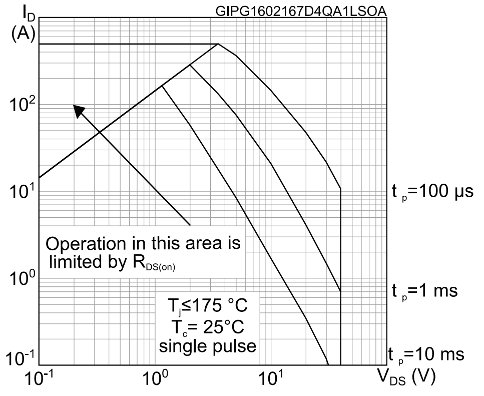



**Figure 3: Thermal impedance**

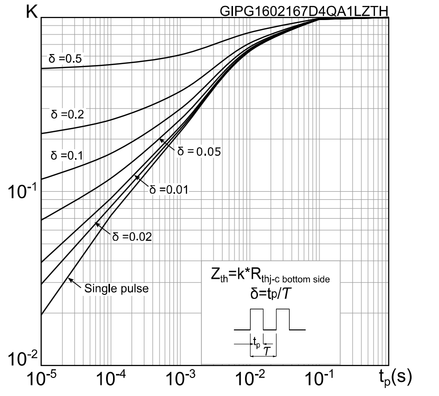



**Figure 4: Output characteristics**

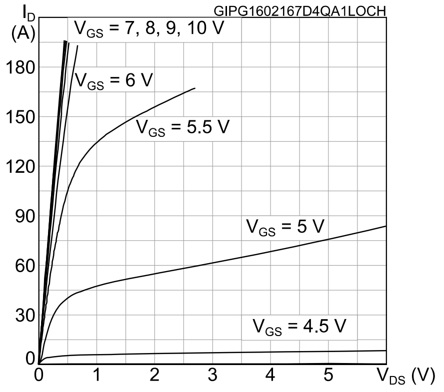



**Figure 5: Transfer characteristics**

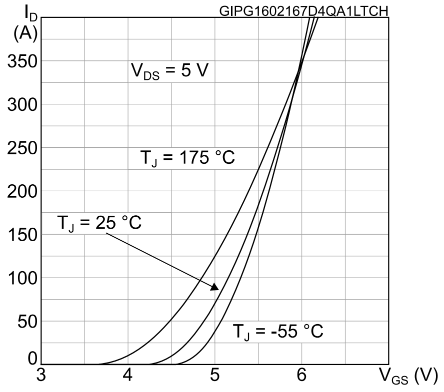



**Figure 6: Gate charge vs gate-source voltage**

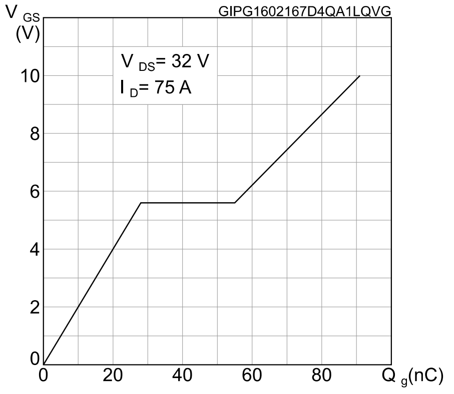



**Figure 7: Static drain-source on-resistance**

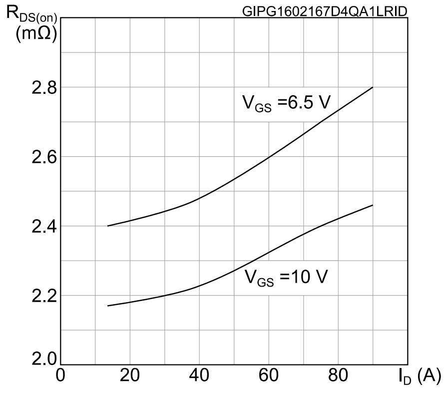


**Figure 8: Capacitance variations**

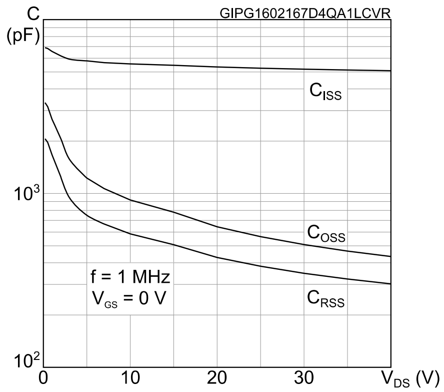



**Figure 9: Normalized gate threshold voltage vs temperature**

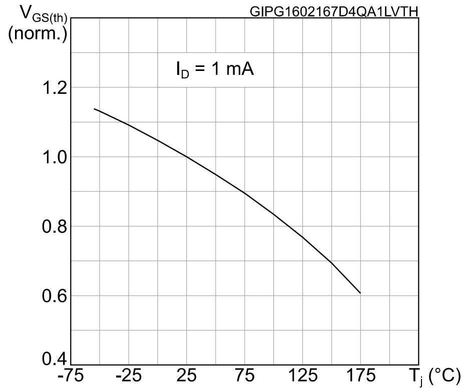



**Figure 10: Normalized on-resistance vs temperature**

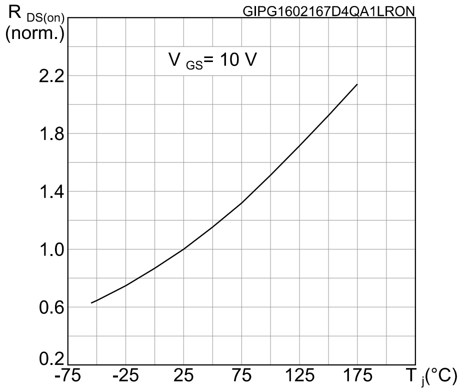



**Figure 11: Normalized V(BR)DSS vs temperature**

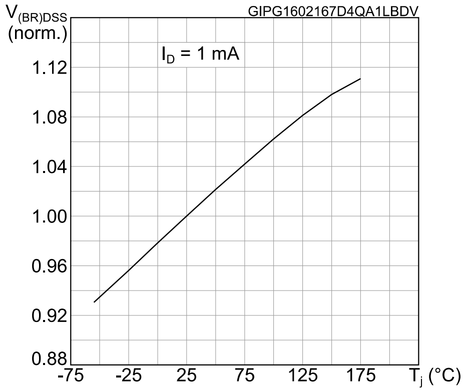
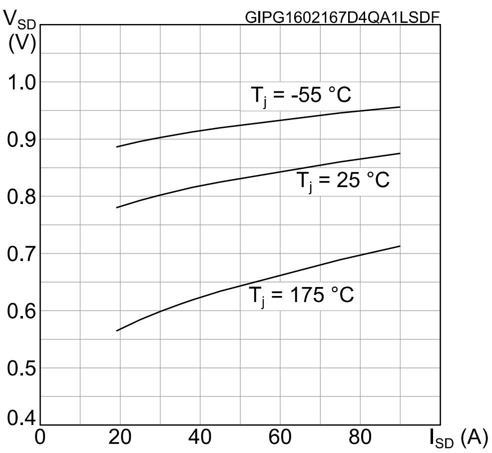



**Figure 12: Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**

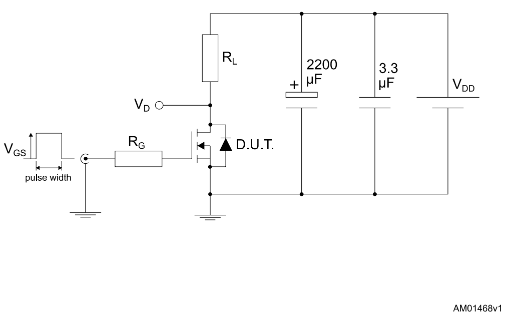



**Figure 14: Test circuit for gate charge behavior**

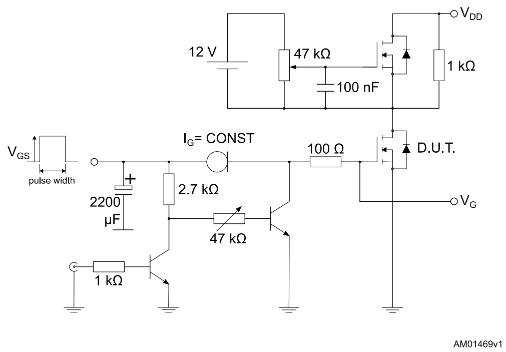



**Figure 15: Test circuit for inductive load switching and diode recovery times**

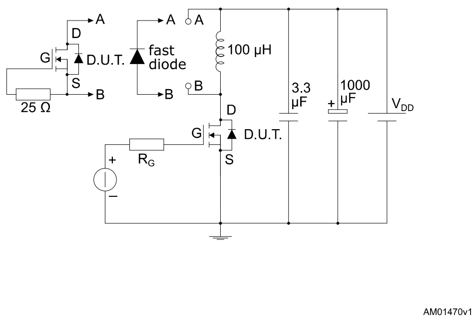



**Figure 16: Unclamped inductive load test circuit**

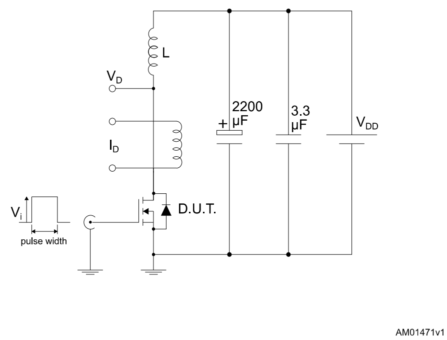



**Figure 17: Unclamped inductive waveform**

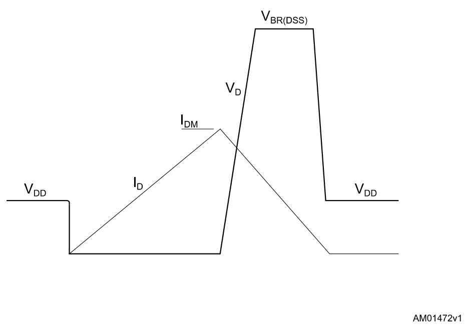
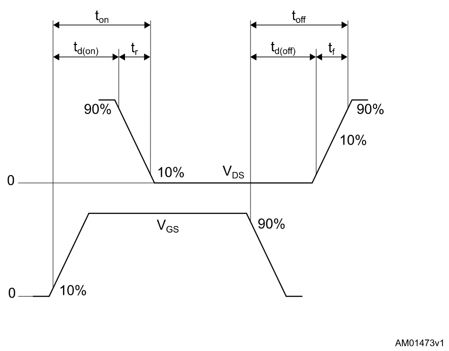



**Figure 18: Switching time waveform**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 4.1 PowerFLAT™ 5X6 dual side cooling package information

**Figure 19: PowerFLAT™ 5x6 dual side cooling package outline**

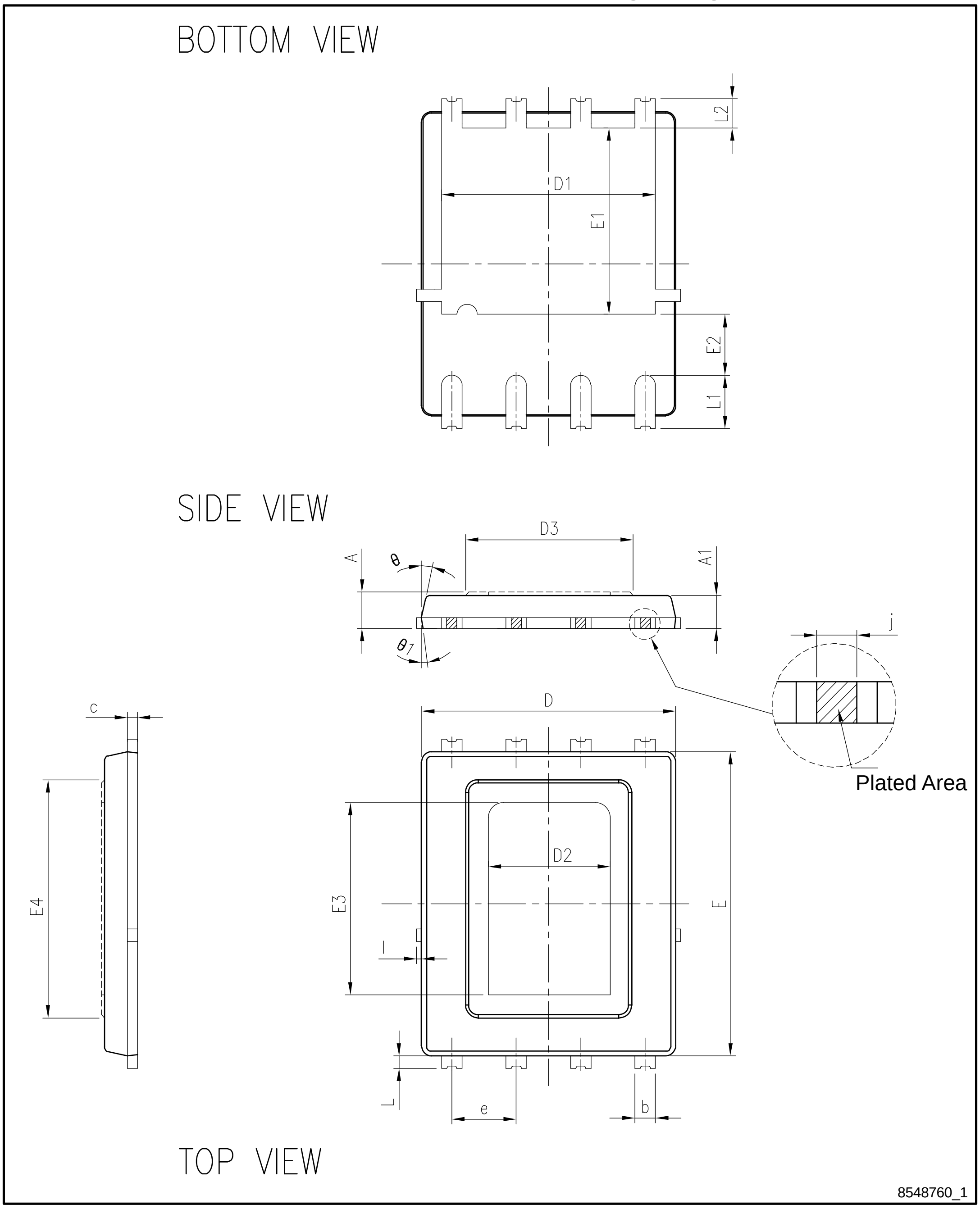
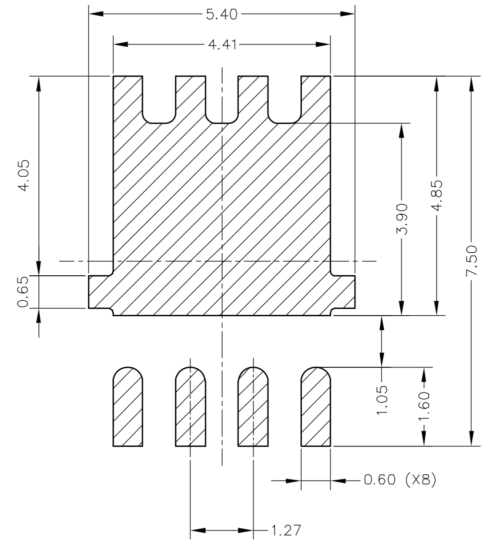


Table 9: PowerFLAT™ 5x6 dual side cooling mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.66 | 0.71 | 0.76 |
| A1 | 0.60 | | 0.75 |
| b | 0.33 | 0.43 | 0.53 |
| c | 0.15 | 0.203 | 0.30 |
| D | 5.00 BSC | | |
| D1 | 4.06 | 4.21 | 4.36 |
| D2 | 2.40 BSC | | |
| D3 | 2.80 | 3.30 | 3.80 |
| E | 6.00 BSC | | |
| E1 | 3.525 | 3.675 | 3.825 |
| E2 | 1.05 | 1.20 | 1.35 |
| E3 | 3.80 BSC | | |
| E4 | 4.20 | 4.70 | 5.20 |
| e | 1.27 BSC | | |
| l | | | 0.15 |
| L | 0.15 | 0.25 | 0.35 |
| L1 | 0.925 | 1.05 | 1.175 |
| L2 | 0.45 | 0.575 | 0.70 |
| ϑ | 12° BSC | | |
| ϑ1 | 7° BSC | | |
| j | 0.20 BSC | | |

Figure 20: PowerFLAT™ 5x6 dual side cooling recommended footprint (dimensions are in mm)



# 5 Revision history

Table 10: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 16-Feb-2016 | 1 | First release. |